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FB2644 VIA Eden Half - Size CPU Card User's Manual

March 2005
Version: 1.4
Part Number: FB2644

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If you have problems or difficulties in using the system board, or setting up the relevant devices, and software that are not explained in this manual, please contact our service engineer for service, or send email to support@fabiatech.com.

Returning Your Board For Service & Technical Support

If your board requires servicing, contact the dealer from whom you purchased the product for service information. You can help assure efficient servicing of your product by following these guidelines:

- A list of your name, address, telephone, facsimile number, or email address where you may be reached during the day
- Description of you peripheral attachments
- Description of you software (operating system, version, application software, etc.) and BIOS configuration
- Description of the symptoms (Extract wording any message)

For updated BIOS, drivers, manuals, or product information, please visit us at www.fabiatech.com

Table of Content

FB2644 VIA Eden Half - Size CPU Card User's Manual i
Table of Content iii
Chapter 1 Introducing the FB2644 System Board 1
Overview 1
Layout 2
Specifications 3
Packing List 4
Chapter 2 Hardware Installation 5
Before Installation 5
Hardware Features 6
SW1 (1,2): Selecting CPU Base Clock and PCI Clock 7
J12&J13: CPU Fan Connector & System Fan Connector 7
J5: Reset Header 8
J8: Power LED Header 8
J1: HDD LED Header 8
CN10, CN11: Keyboard/Mouse Connector 9
J3: USB Connector 9
CN7, J7: RJ45 LAN Connector 10
CN1, CN2: IDE hard Disk Connector 10
DB2, CN9: RS232 Serial Ports 1,2 Connectors and Jumpers 11
J6: Temperature Sensor Header 13
CN4: 26-pin Parallel Port Connector 14
CN3: Floppy Connector 15
BZ1& J15: On-Board Buzzer & External Speaker Header 15
JP3: CMOS Data Clear Jumper 16
On-Board Power and Watchdog LED (LED1) 16

J17: Power Connector (6-pin 2.54mm JST) 17
J16, J2 & JP4: Soft Start Connector (*for ATX Power Supply Only*) 17
J4: TTL I/O Connector 18
DIMM1: SoDIMM Socket 18
J18 & JP1: Compact Flash Socket and Master/Slave Select 18
J10: AMR Connector 19
Chapter 3 Installing CRT 21
LCD FLAT PANEL DISPLAY 21
CRT & LCD DISPLAY 22
CN5, CN6 & CN8: LCD Connector and Power connector 23
Chapter 4 BIOS Setup 25
Overview 25
BIOS Functions 26
Keyboard Convention 27
STANDARD CMOS SETUP 28
ADVANCED CMOS SETUP 30
ADVANCED CHIPSET SETUP 35
POWER MANAGEMENT 38
PCI/PLUG AND PLAY 41
PERIPHERAL SETUP 44
Hardware Monitor Setup 48
Password Setup 49
Chapter 5 Driver and Utility 51
VGA/Audio Driver for WIN98/WIN95 51
BIOS Flash Utility 52
LAN Utility 52
Watchdog Timer 53
Watchdog Timer Setting 54
Watchdog Timer Enabled 55
Watchdog Timer Trigger 55
Watchdog Timer Disabled 55
Programming RS-485 56
Chapter 6 Technical Reference 61
Trouble Shooting for Error Messages 61

Technical Reference 64
Real-Time Clock and Non-Volatile RAM 64
CMOS RAM Map 66
I/O Port Address Map 67
Interrupt Request Lines (IRQ) 68
DMA Channel Map 69
DMA Controller 2 69
Serial Ports 70
Parallel Ports 74
Appendix 77
Dimension 77
Special Features 78
J9: Feature Connector (J9: 44-pin 2.0mm IDC) 78

Chapter 1 Introducing the FB2644 System Board

Overview

The FB2644 is a VIA Eden Low power processor, all in one, half-size PCI CPU card. This user's manual provides information on the physical features, installation, and BIOS setup of the FB2644.

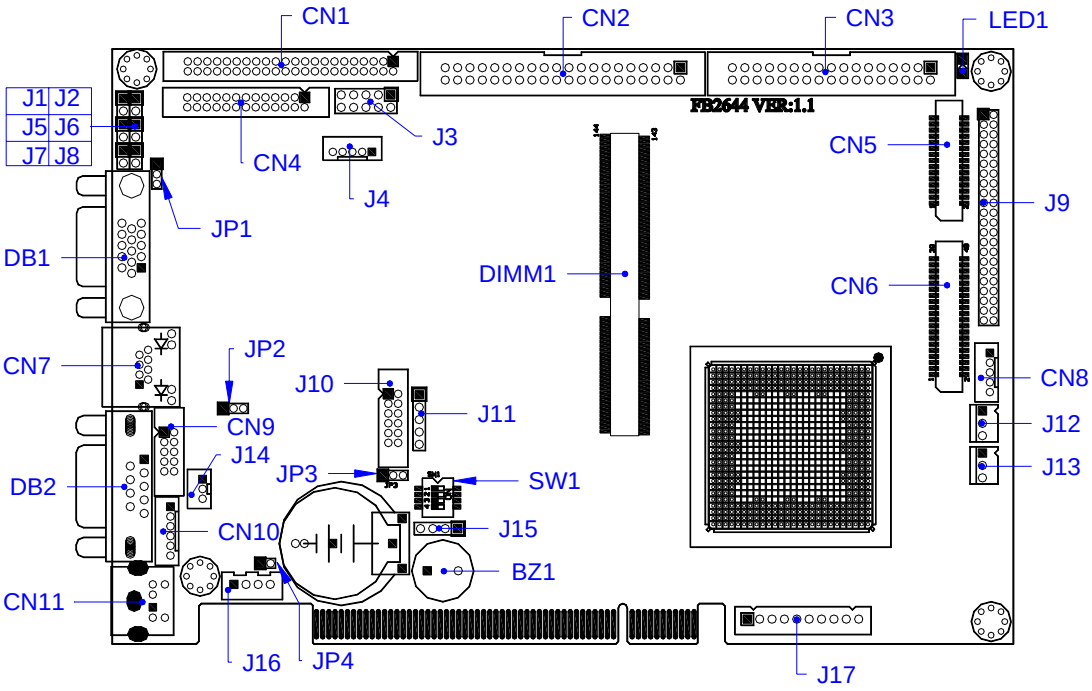
Built to unleash the total potential of the VIA Eden Processor, the FB2644 is a single boards computer capable of handling today's demanding requirements. Able to support 300MHz ~1 GHz CPUs, this unit supports 10/100M interface network port, synchronous pipeline burst SDRAM up to 578MB and a onboard VGA port up to 32MB share memory that can support TTL/LVDS LCD's and CRT's simultaneously or independently.

Each FB2644 has two ports for I/O communications. One RS-232C and one RS-232 /422/485 ports are available. There is also a watchdog timer that can be configured from software to automatically reset the system or generate an interrupt if there is a system's or EMI problem. And for easy configuration, AMI BIOS are available.

Power management is also featured to lower the rate of consumption. The unit supports doze mode, <Suspend Mode> and <Standby mode> as well as it adheres to the "Green Function" standard.

The FB2644 is perfect for POS and POI applications, network systems, panel / MMI's, order entry kiosks, test equipment, OEM projects or as a motherboard for a panel PC. The unit is only 185X122mm, offering unparalleled performance in a very small footprint.

Layout


CN1
CN2
CN3
LED1
J1 J2
J5 J6
J7 J8
FB2644 VER:1.1
J3
CN4
J4
CN5
J9
JP1
DB1
DIMM1
CN6
JP2
CN7
J10
CN8
J11
CN9
J12
J14
JP3
SW1
DB2
J13
CN10
J15
BZ1
CN11
J16
JP4
J17

Specifications

- Supports 300MHz ~1GHz Low Power CPU. (VIA Eden CPU)
- Compact size slot card with PICMG PCI expansion bus.
- VIA VT8606+VT82C696B chipset and 64KB or above L2 cache inside the CPUs.
- On-board 64MB SDRAM and 1 SoDIMM socket for up to 576MB maximum.
- 100M/10M Ethernet with RJ-45 connector.
- Onboard VGA port (VT8606 embedded) supports CRT, TTL/LVDS LCD with up to 32MB shared memory.
- Parallel port, floppy and support two Enhanced IDE channels.
- One RS-232 and One RS-232/RS-422/RS-485/IrDA.
- PS/2 compatible keyboard and mouse interface.
- Optional Compact Flash socket for 3.3V Compact Flash and Micro Drives.
- E2KEY function for safe CMOS data keeping. (Option)
- On-board buzzer and LED indicator.
- Software programmable watchdog timer.
- Two USB ports and hardware monitoring functions.
- Provides two CPU & case cooling fan connector for monitoring.
- Provides One AC97 and One feature connector for ***Audio***, and ***Video In/Out*** solutions. (Optional).
- Flash BIOS with easy upgrade utility.
- Compact size, 185 mm x 122 mm.

Packing List

Upon receiving the package, verify the following things. Should any of the mentioned happens, contact us for immediate service.

- Unpack and inspect the FB2644 package for possible damage that may occur during the delivery process.
- Verify the accessories in the package according to the packing list and see if there is anything missing or incorrect package is included.
- If the cable(s) you use to install the FB2644 is not supplied from us, please make sure the specification of the cable(s) is compatible with the FB2644 system board.

Note: after you install the FB2644, it is recommended that you keep the diskette or CD that contains drivers and document files, document copies, and unused cables in the cartoon for future use.

The following lists the accessories that may be included in your FB2644 package. Some accessories are optional items that are only shipped upon order.

- One FB2644 system board
- One compact disc containing manual file in PDF format and necessary drivers and utilities
- One 40-pin hard disk drive interface cable
- One 34-pin floppy drive interface cable
- One serial port and parallel port interface cable with bracket
- One mouse port adapter cable with bracket
- One hard copy of Quick Installation Guide
- One 2-port USB adapter cable (Optional)

Chapter 2 Hardware Installation

To set up a FB2644 system board, complete the description Chapter 2 and Chapter 3.

This chapter introduces the system board connectors, jumper settings and then guides you to apply them for field application.

Before Installation

Before you install the system board, make sure you follow the following descriptions.

1. Before removing the board from its anti-static bag, wear an anti-static strap to prevent the generation of Electricity Static Discharge (ESD). The ESD may be created from human body that touches the board. It may do damage to the board circuit.

2. Install or unplug any connector, module, or add-on card, be sure that the power is disconnected from the system board. If not, this may damage the system board components, module, or the add-on-card.

3. Installing a heat sink and cooling fan is necessary for heat dissipation from your CPU. If heat sink or cooling fan is not mounted, this may cause the CPU fail due to over-heating problem.

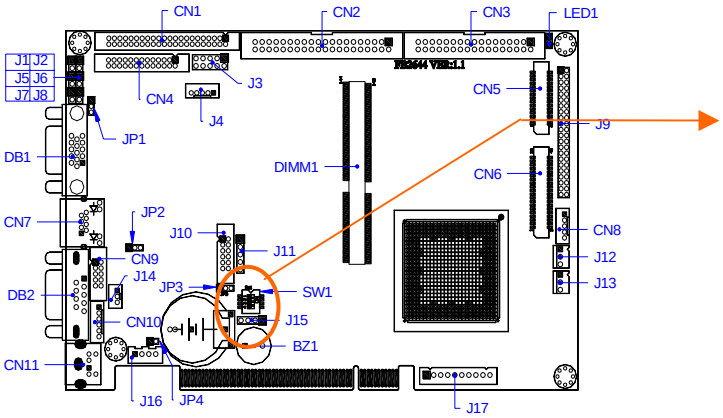
4. When you connect the connectors and memory modules, be careful with the pin orientations.

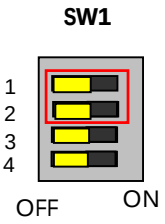
Hardware Features

The following lists the connectors and jumpers to install the FB2644.

Item	Description
CN1	44-pin 2.0mm IDE 2 hard disk connector
CN2	40-pin 2.54mm IDE 1 hard disk connector
CN3	34-pin 2.54mm floppy connector
CN4	26-pin 2.0mm parallel port connector
CN5	LCD Connector with 36 bit LVDS signals
CN6	LCD Connector with 24 bit TTL signals
CN7	RJ45-Lan connector
CN8	For Inverter connector
CN9	10-pin RS-232 port 2 connector
CN10, CN11	Keyboard and Mouse connector
J1	2-pin HDD LED Indicator header
J2	ATX soft power switch header
J3	USB connector
J4	5-pin for TTL I/O
J5	2-pin Reset header
J6	2-pin for external temperature sensor
J7	2-pin for external TX-LED with LAN
J8	2-pin for External power / watchdog LED header
J9	Feature Connector External Bus for Piggyback place with Video In/Out
BZ1, J10	AMR connector for provides AC97 signals for Audio and Modem functions
J11	5-pin RS232C IrDA header for serial port 2
J12, J13	3-pin for case/CPU cooling fan
J14	3-pin RS232C touch screen header for serial port 2
J15	Onboard Buzzer and external speaker header
J16, JP4	Soft start connector for AXT power supply only
J17	9-pin power connector
J18, JP1	Compact Flash Socket and Master/Slave Select
JP2	Terminator for RS422/RS485
JP3	To clear CMOS data
DB1	CRT connector
DB2	RS232 9-pin D – type male connector
LED1	Power and watchdog of LED indicator
SW1	To selects CPU base clock and PCI clock and RS232/RS422/RS485

□ SW1 (1,2): Selecting CPU Base Clock and PCI Clock



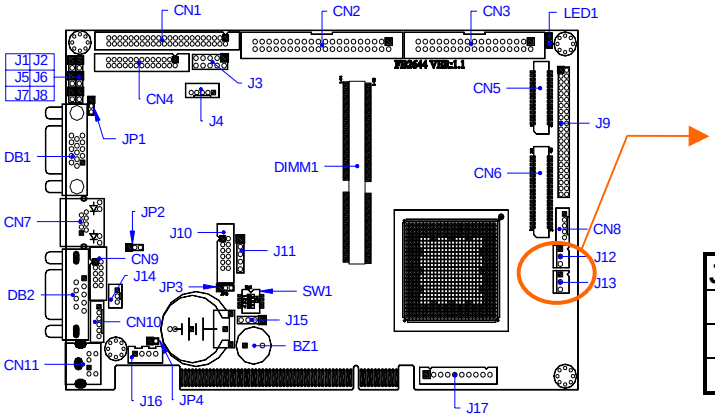


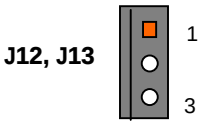
The following lists the switch settings of CPU Base Clock and PCI clock.

SW1-1	SW1-2	CPU Base Clock	PCI Clock	Remark
Off	Off	133.0MHz	33.3MHz	Default
Off	On	100.0Mhz	33.3Mhz	
On	Off	105.0Mhz	33.3Mhz	
On	On	66.7Mhz	33.3Mhz	

✧ Caution (*1): Avoid any of the following conditions that will directly destroy or severely cause damage to your CPU, or make your system unstable if you select an inappropriate base clock.

□ J12&J13: CPU Fan Connector & System Fan Connector

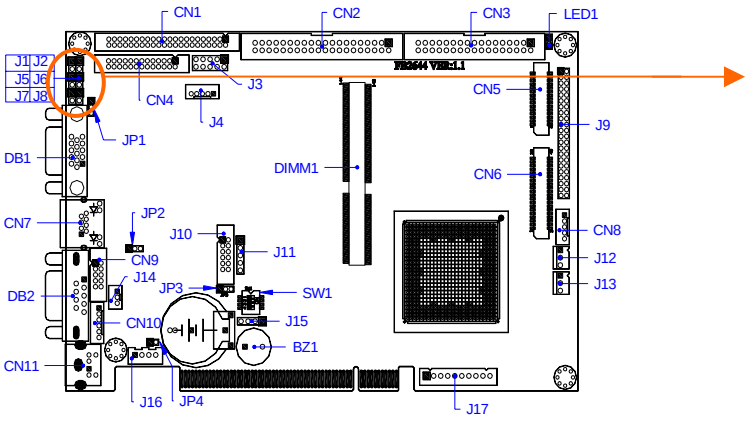




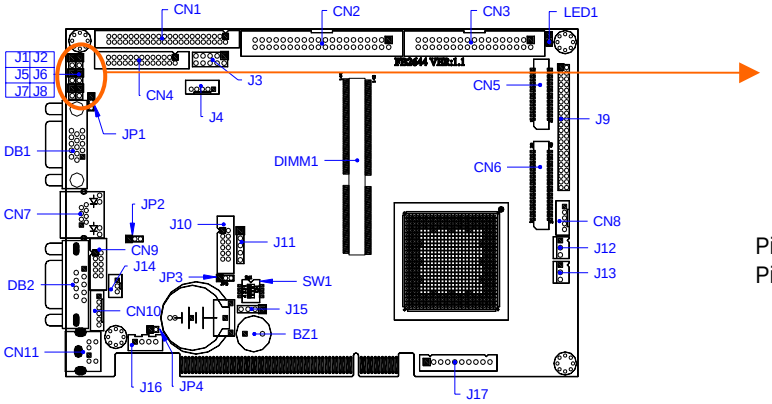
J12&J13	Description
1	Ground
2	+12V
3	Speed-In

□ J5: Reset Header

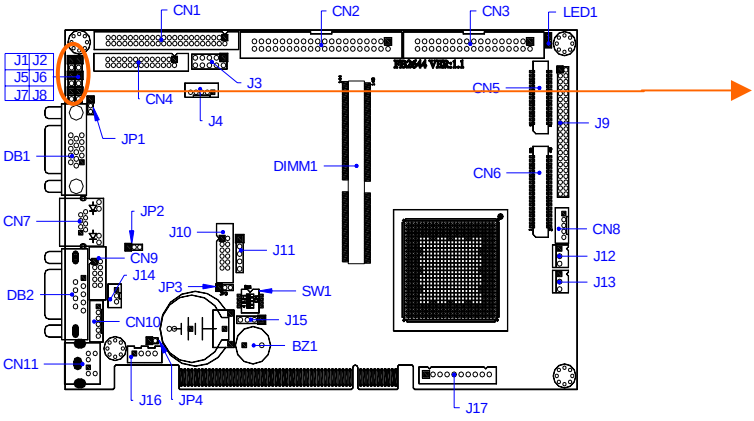
J5 is a 2-pin header for connecting to system reset bottom. Short-circuit these 2 pins to hardware reset FB2644 as well as restart system. It is similar to power off the system and then power it on again.



□ J8: Power LED Header

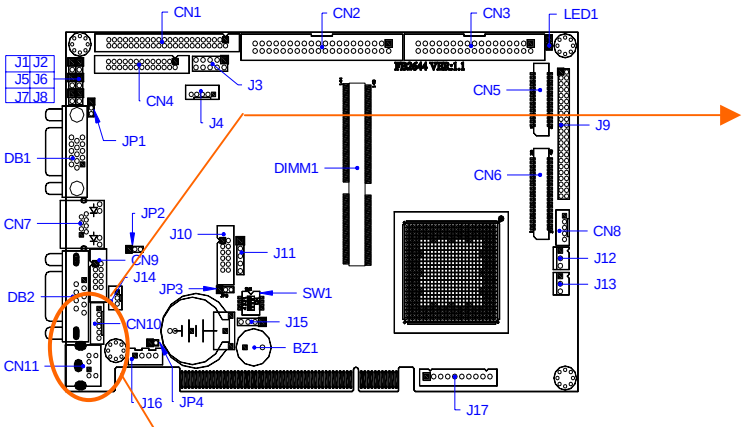


□ J1: HDD LED Header



□ CN10, CN11: Keyboard/Mouse Connector

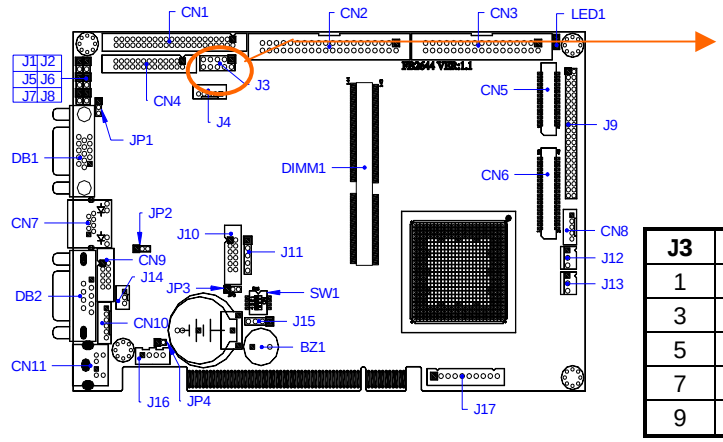
CN11 is a standard PS/2 type keyboard connector, so any PS/2 type keyboard can plug into directly without extra adapter cable. CN10 provides PS/2 mouse interface, use the included mouse adapter cable to connect between CN8 and standard PS/2 mouse.



CN10	CN11	Signal
1	2	Mouse Data
2	1	Keyboard Data
3	3	Ground
4	4	VCC
5	6	Mouse Clock
6	5	Keyboard Clock

□ J3: USB Connector

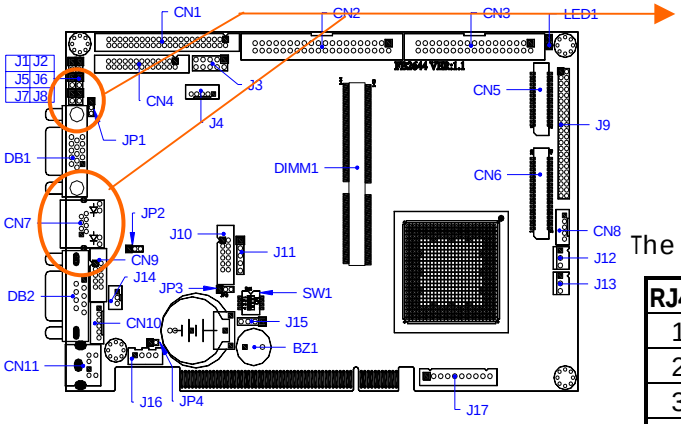
J3 is a 10-pin connector. Use included adapter cable (Optional) for transfering to standard double port USB connector. The upper port is USB #0 and the lower port is USB#1

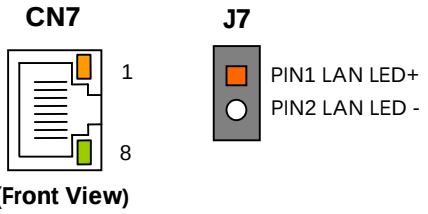


J3	Signal	J3	Signal
1	USBV0	2	Case Ground
3	USBD0-	4	USBG1
5	USBD0+	6	USBD1+
7	USBG0	8	USBD1-
9	Case Ground	10	USBV1

□ CN7, J7: RJ45 LAN Connector

The CN7 contain LAN twist pair signals and LAN accesses indicator signal is RJ45 type connector with 2 LED indicators. The up side LED (orange) indicates data is accessing and the down side LED (green) indicates on-line status. (When lighted indicates on-line and off indicates off-line). The following lists the pin assignment of CN7 and J7:



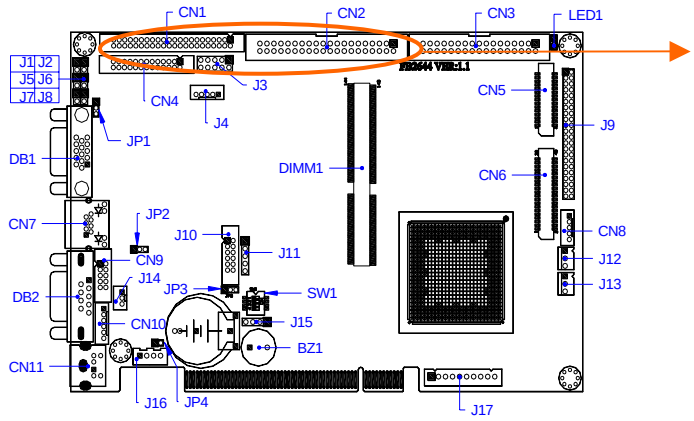


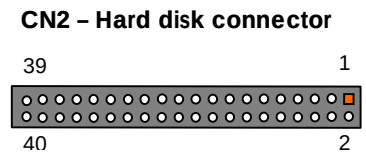
The following lists the pin assignment of RJ45.

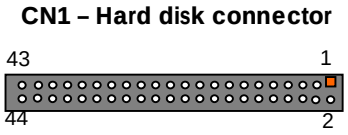
RJ45	Signal	RJ45	Signal
1	TPTX+	5	FBG1
2	TPTX -	6	TPRX -
3	TPRX+	7	FBG2
4	FBG1	8	FBG2

□ CN1, CN2: IDE hard Disk Connector

CN 2 is 40-pin 2.54mm IDE hard disk connector. CN1 is 44-pin 2.0mm IDC connectors. The PCI IDE interface has two enhanced IDE channels and supports 4 IDE devices with ultra DMA 33 and or IDE channel 1 IDE supports ultra DMA 33/66/100.







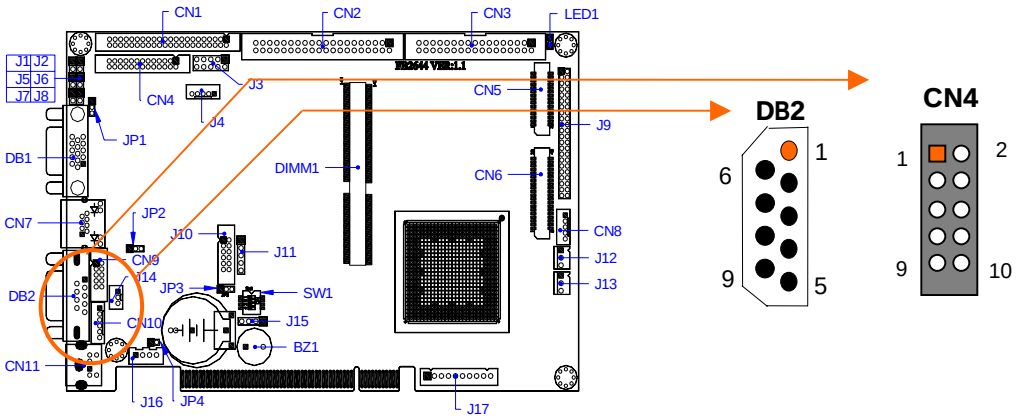
✧ Caution: If you use ULTRADMA/66/100 devices, you will need to purchase another UltraDMA/66/100 cable. UltarDMA/66/100 IDE devices must use a 40-pin 80-conductor IDE cable. (See P44 PERIPHERAL SET UP)

The following table lists the pin description of CN1, CN2.

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	IDEDREQ	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	IDEIORDYA	28	GROUND
29	-DACKA	30	GROUND
31	AINT	32	GROUND
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND
41 (CN1)	VCC	42 (CN1)	VCC
43 (CN1)	GROUND	44 (CN1)	Not Used

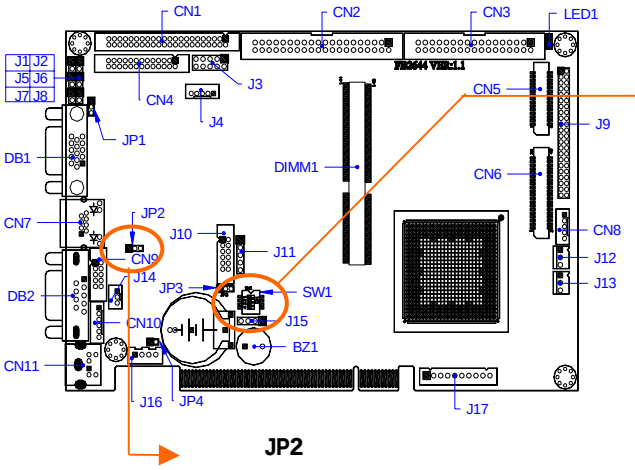
□ DB2, CN9: RS232 Serial Ports 1,2 Connectors and Jumpers

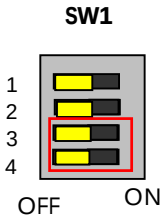
The DB2 connector on bracket is 9-pin D-type male connector the serial port 2 adapter cables are used to transfer 10-pin IDC connector into standard DB9 connectors.



❑ Serial Port 2 (CN9, SW1, J11, J14 and JP2)

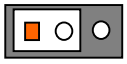
Serial port 2 is designed for multiple proposes. It could be RS-232C, RS-422 or RS-485 by selecting SW1 or changing the setting in BIOS setup program, and JP2 is use to enable or disable terminator if RS-485 mode is selected. Serial port 2 also could be configured as Infra (IrDA) interface by changing the setting in BIOS setup program. J11 is use to interface with Infra module. When touch screen module is used, you could connect J14 to touch screen controller directly and internally instead of connect from CN9 connector.



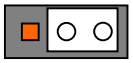


SW1-3	SW1-4	Signal
Off	Off	RS-232
Off	On	RS-485
On	Off	RS-422
On	On	Software*

Factory Preset: RS232
*Note: Changing the setting in BIOS setup program



Pin 1,2 Close: Terminator Enabled

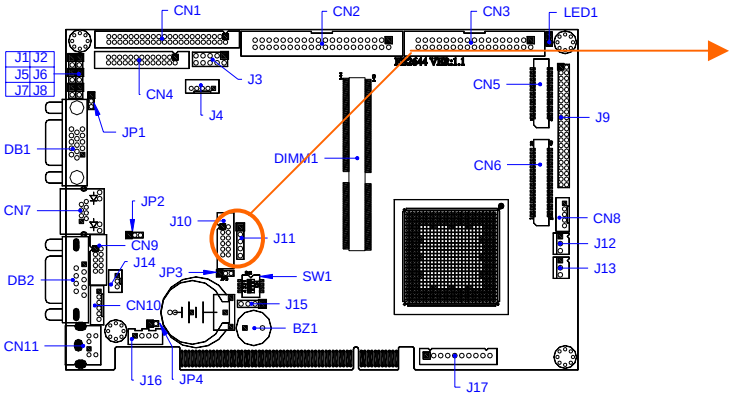


Pin 2,3 Close: Terminator Disable
Default

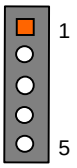
CN9	Signal	RS422	RS485	DB9
1	-DCD2			1
2	-DSR2			6
3	RXD2	RX-	485-	2
4	-RTS2	TX-		7
5	TXD2	RX+	485+	3
6	-CTS2	TX+		8
7	-DTR2			4
8	-RI2			9
9	GROUND			5
10	CASE GROUND			

❑ J11: 5-pin Infrared Header

J11 provides infrared signals of serial port 2. The infrared signal is used to interface with Infrared modules.



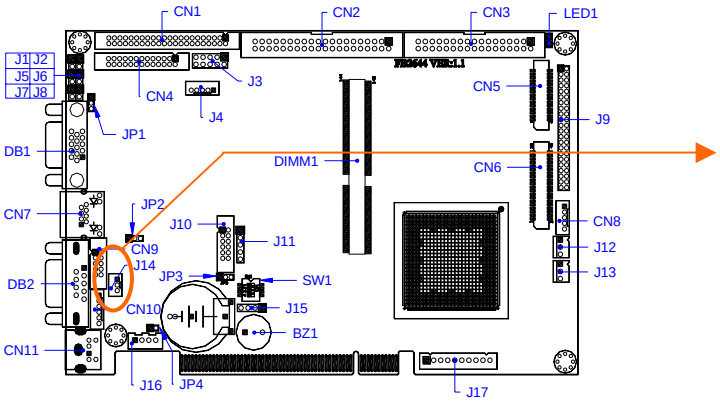
J11



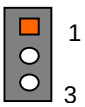
Pin 1: VCC
Pin 2: N.C.
Pin 3: IRRX
Pin 4: Ground
Pin 5: IRTX

❑ J14: Touch Screen Header

J14 provide basic RS-232C signals of serial port 2 respectively. The basic RS-232C signal is used to interface with touch screen controller internally.

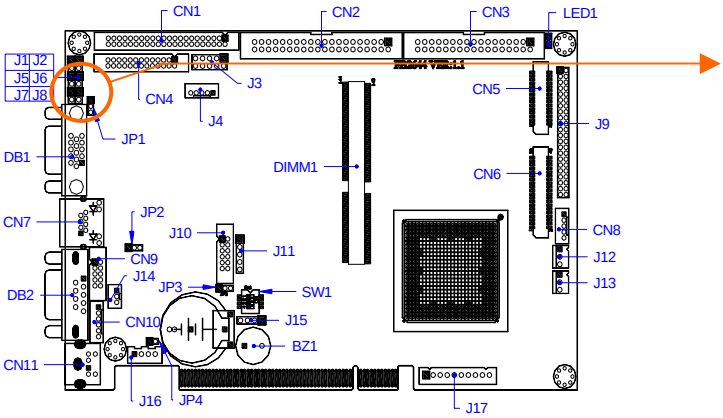


J14

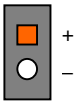


Pin 1: TXD
Pin 2: RXD
Pin 3: Ground

❑ J6: Temperature Sensor Header



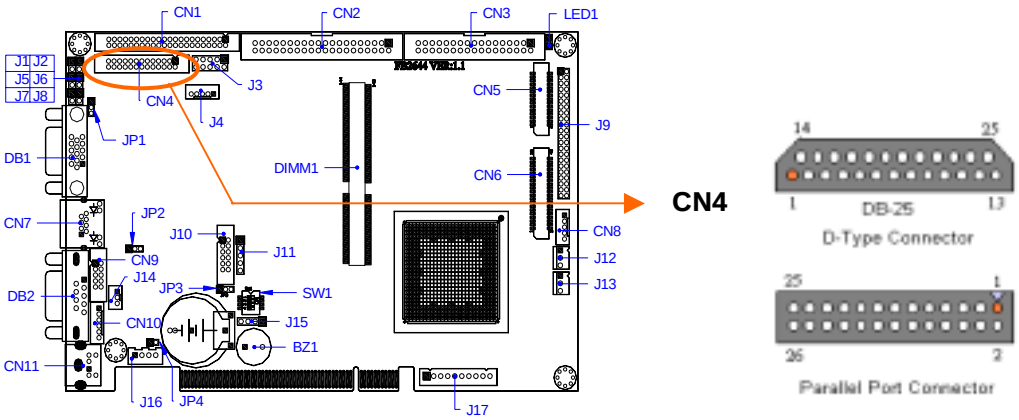
J6



Resistive Temperature Sensor Input Header

□ CN4: 26-pin Parallel Port Connector

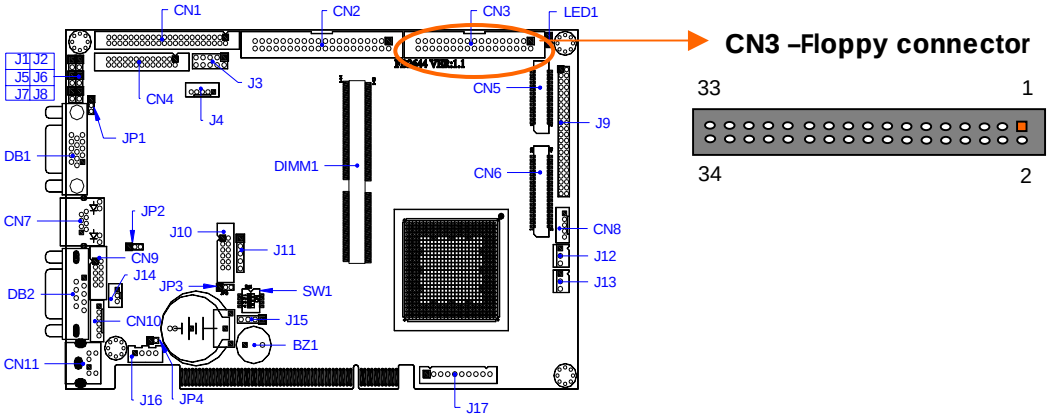
The included printer interface cable is used to transfer 26-pin connector into standard DB25 connector.



CN4	DB-25	Signal	CN4	DB-25	Signal
1	1	-STROBE	2	14	-AUTO FORM FEED
3	2	DATA 0	4	15	-ERROR
5	3	DATA 1	6	16	-INITIALIZE
7	4	DATA 2	8	17	-PRINTER SELECT IN
9	5	DATA 3	10	18	Ground
11	6	DATA 4	12	19	Ground
13	7	DATA 5	14	20	Ground
15	8	DATA 6	16	21	Ground
17	9	DATA 7	18	22	Ground
19	10	-ACKNOWLEDGE	20	23	Ground
21	11	BUSY	22	24	Ground
23	12	PAPER	24	25	Ground
25	13	PRINTER SELECT	26	--	No Used

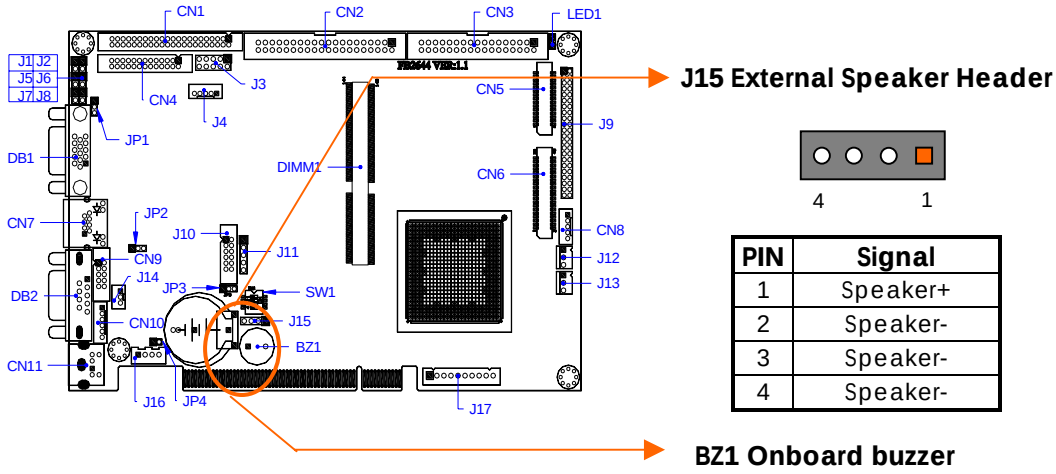
□ CN3: Floppy Connector

The included floppy drive interface cable is used standard 34-pin connector. The following table shows signal connections 34-pin connectors.



34-pin	Signal	34-pin	Signal
2	Drive Enable A	23	Ground
8	-Index	24	-Write Enable
12	-Select A	26	-Track 0
11	Ground	28	-Write Protect
16	-Motor A	29	Ground
14	- Select B	30	-Read Data
10	-Motor B	31	Ground
9	Ground	32	-Head
18	-Direction	33	NC
20	-Step	34	-Disk Change
22	-Write Data	Others	No Connection

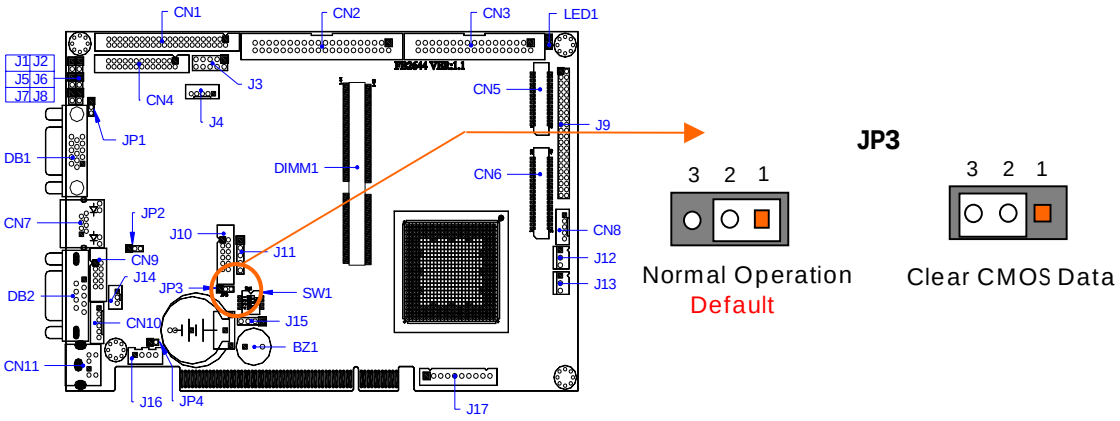
□ BZ1& J15: On-Board Buzzer & External Speaker Header



PIN	Signal
1	Speaker+
2	Speaker-
3	Speaker-
4	Speaker-

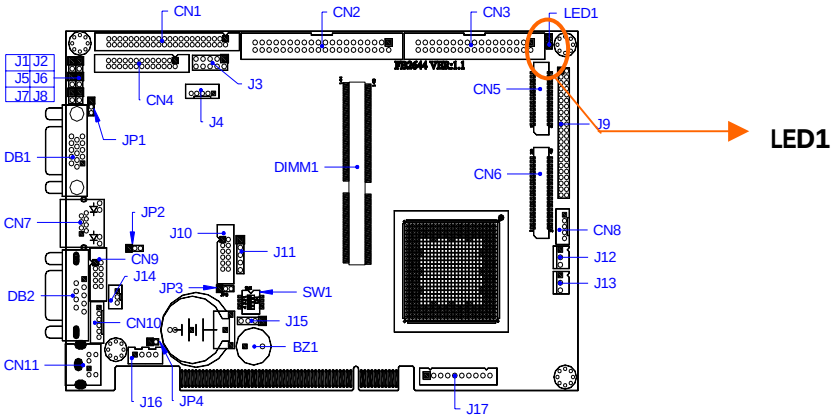
□ JP3: CMOS Data Clear Jumper

You can use JP3 to clear CMOS data. The CMOS store information like system date, time, boot up device, password, IRQ... that are set up with the BIOS. To clear the CMOS, set JP1 to 2-3 and then return to 1-2. The default setting is 1-2.



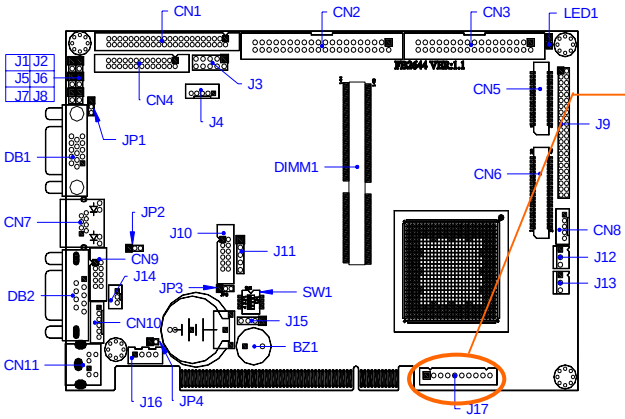
□ On-Board Power and Watchdog LED (LED1)

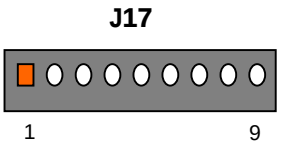
LED1 indicates power is active when it lights. If the watchdog is enabled, LED1 will blink in a stable period.



□ J17: Power Connector (6-pin 2.54mm JST)

J17 is the power connector for FB2644 is used with stand-alone applications.



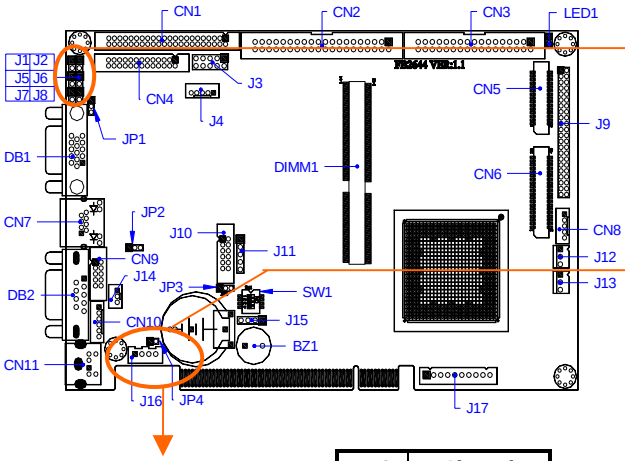


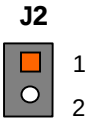
Note:This power connector is ideal for standalone applications.

J17	Signal	J17	Signal
1	+5V	6	Ground
2	+5V	7	Ground
3	Ground	8	+5V
4	Ground	9	+5V
5	+12V		

□ J16, J2 & JP4: Soft Start Connector (*for ATX Power Supply Only*)

When ATX power supply is used, you can connect J16 to ATX control signals from the back plane, and connect J2 to a push bottom switch as soft power switch. If non-ATX power supply is used, please short JP4 with jumper and you don't need to connect J16 and J2.

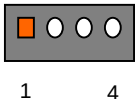




ATX Soft Power Switch Header

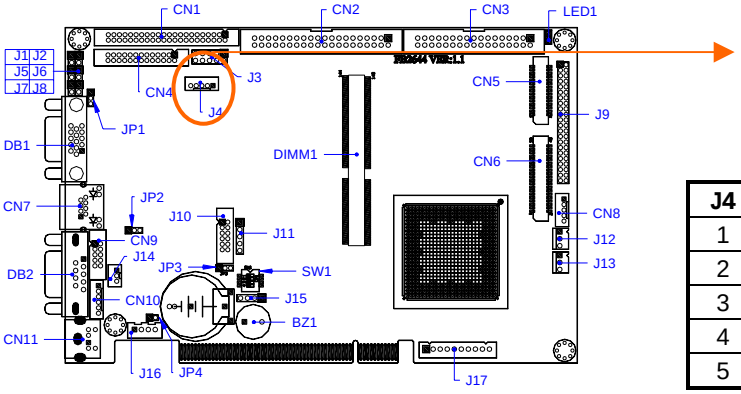
Close: Non - ATX Power
Default

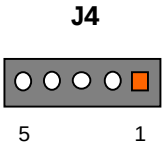
Open: ATX Power



J16	Signal
1	Ground
2	PSON#
3	Power OK
4	VCCSB

□ J4: TTL I/O Connector

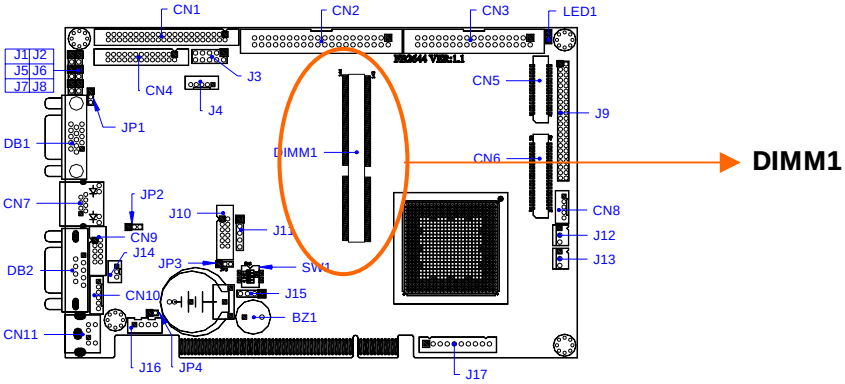




J4	TTL Lines	Bit Location
1	Output Line 0	Bit 4 of 84eh
2	Output Line 1	Bit 5 of 84eh
3	Input Line 0	Bit 4 of 84ah
4	Input Line 1	Bit 5 of 84ah
5	Ground	-

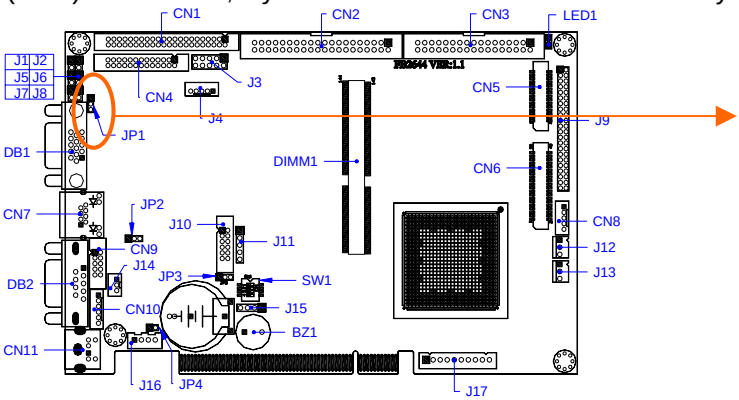
□ DIMM1: SoDIMM Socket

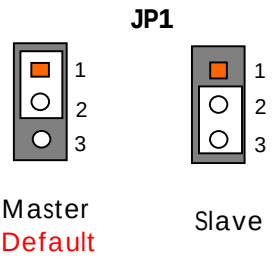
DIMM1 supports 144-pin, 3.3V, and PC-133 SDRAM with size of 32MB, 64MB, 128MB, 256MB and 512MB.



□ J18 & JP1: Compact Flash Socket and Master/Slave Select

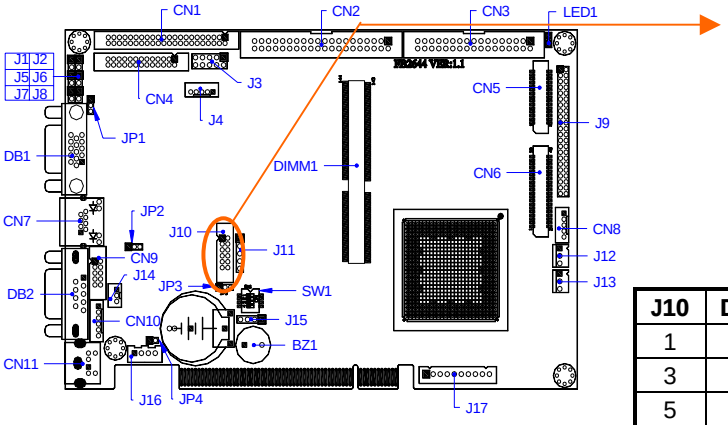
The Compact Flash socket J18 (on the solder side) is optional and supports 3.3V Compact Flash and Micro Drives. JP1 is used to select master/slave device of this socket. Be sure to avoid the same master/slave setting with which connects to IDE#2 (CN1) connector, if you use J18 and CN1 simultaneously.

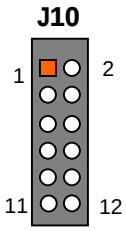




□ J10: AMR Connector

J10 provides AC97 signals for Audio and Modem functions. FB4641 (Audio Adapter Board, Optional) is recommended for your best Audio solutions.





J10	Description	J10	Description
1	BITCLK	2	+12v
3	+5V	4	SYNC
5	Ground	6	Ground
7	+3.3V	8	ACRST#
9	SDOUT	10	SPKR
11	SDIN	12	SDIN2

Chapter 3 Installing CRT

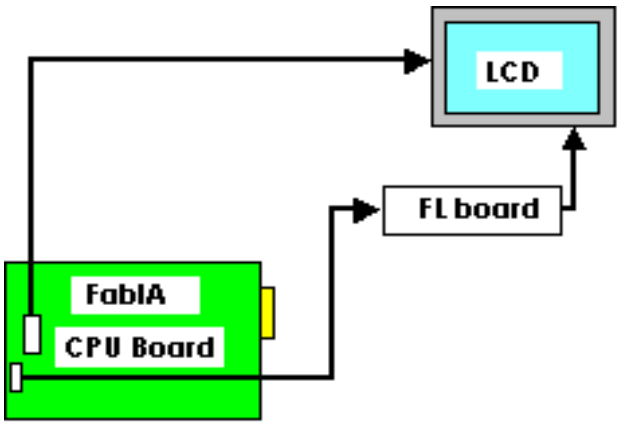
This chapter describes the configuration and installation procedure of LCD and CRT displays. Both CRT and LCD displays may be used at the same time. However, each type of LCD requires different BIOS. This section describes the configuration and installation procedure using LCD display. Skip this section if you are using CRT monitor only.

- LCD Flat Panel Display
- CRT & LCD Display

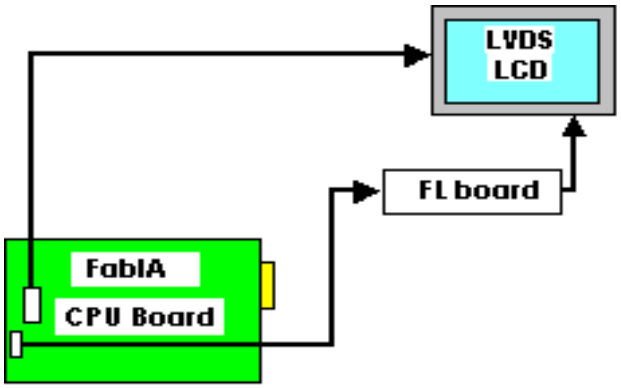
LCD FLAT PANEL DISPLAY

Using the BIOS setting for different types of LCD panel. And then set your system properly and configure BIOS setting for the right type of LCD panel you are using.

The following shows the block diagram of using FB2644 for LCD display.



LCD Panel Block Diagram



LVDS/Panel Link Diagram

The block diagram shows that FB2640 till needs components to be used with a LCD panel.

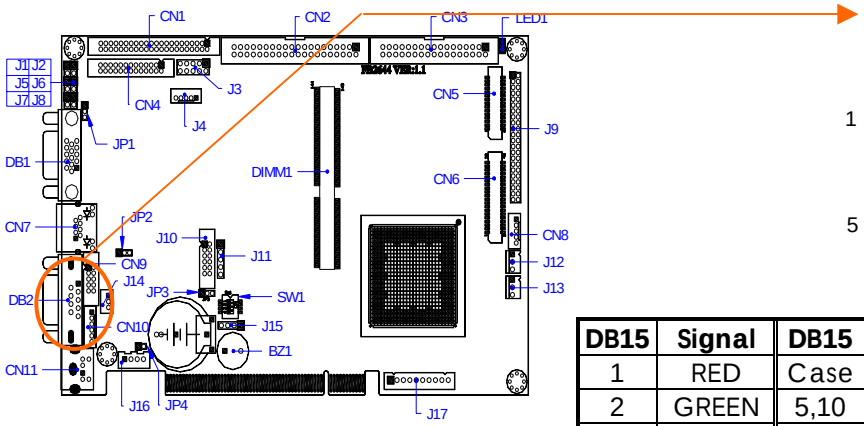
NOTE: Be careful with the pin orientation when installing connectors and the cables. A wrong connection can easily destroy your LCD panel. The pin 1 of the cable connectors is indicated with a sticker and the pin1 of the ribbon cable usually has a different color.

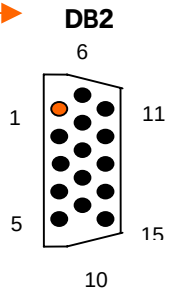
CRT & LCD DISPLAY

The FB2644 supports a CRT colored monitor and a LCD. It can be connected to create a compact video solution for the industrial environment. 32MB simulated VRAM allows a maximum CRT resolution of 1600X1200 with 64K colors.

DB2: CRT connector

The CRT is use to a standard CRT connector (DB2).

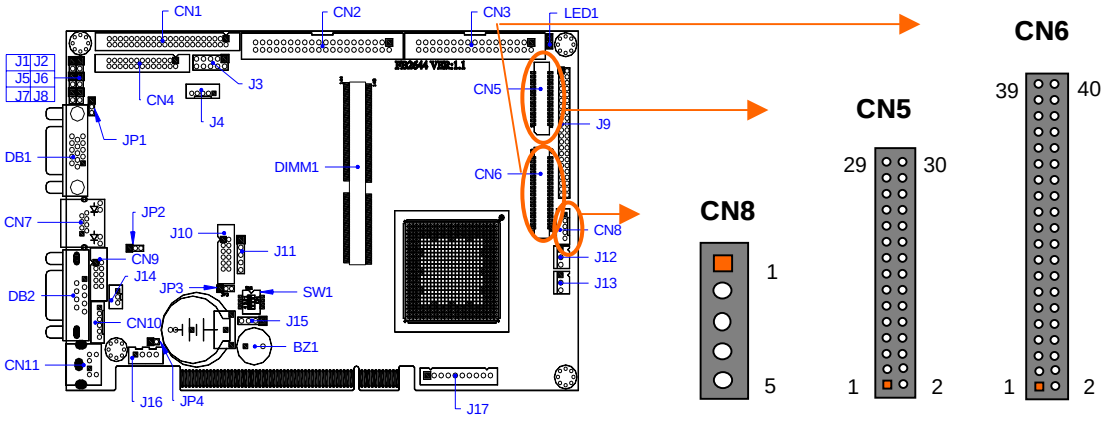




DB15	Signal	DB15	Signal
1	RED	Case	Case Ground
2	GREEN	5,10	Digital Ground
3	BLUE	6,7,8	Analog Ground
14	VSYNC	15	DDC Clock
13	HSYNC	12	DDC Data

CN5, CN6 & CN8: LCD Connector and Power connector

CN6 supports 24-bit TTL LCD signals, CN5 supports 36-bit (2 Channel) LVDS LCD signals, and CN8 is the power connector for inverter board.



Pin	CN6	CN5	Pin	CN6	CN5
1	+5V	Ground	2	+5V	Y0+
3	Ground	Y0-	4	Ground	Ground
5	+3.3V	Y1+	6	+3.3V	Y1-
7	NC	Ground	8	Ground	Y2+
9	FP0	Y2-	10	FP1	Ground
11	FP2	YCK+	12	FP3	YCK-
13	FP4	Ground	14	FP5	Z0+
15	FP6	Z0-	16	FP7	Ground
17	FP8	Z1+	18	FP9	Z1-
19	FP10	Ground	20	FP11	Z2+
21	FP12	Z2-	22	FP13	Ground
23	FP14	ZCK+	24	FP15	ZCK-
25	FP16	Ground	26	FP17	Ground
27	FP18	+3.3V	28	FP19	+3.3V
29	FP20	+5V	30	FP21	+5V
31	FP22		32	FP23	
33	Ground		34	Ground	
35	SHFCLK		36	FP (VS)	
37	DE		38	LP (HS)	
39	ENVDD		40	ENAVEE	

Pin	CN8
1	+12 V
2	GND
3	ENABLK
4	N.C
5	+5 V

Note: If any trouble when connecting FB2644 with LCD panels, you could contact technical support division of FablATech Corporation.

Chapter 4 BIOS Setup

This chapter describes the BIOS setup.

Overview

BIOS are a program located on a Flash memory chip on a circuit board. It is used to initialize and set up the I/O peripherals and interface cards of the system, which includes time, date, hard disk drive, the PCI bus and connected devices such as the video display, diskette drive, and the keyboard. This program will not be lost when you turn off the system.

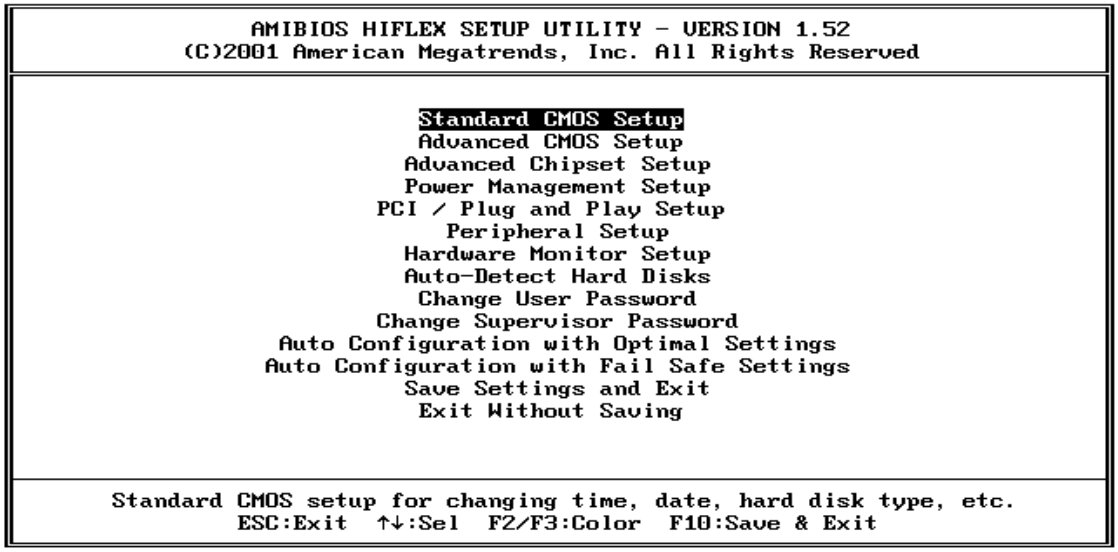
The BIOS provides a menu-driven interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

All the changes you make will be saved in the system RAM and will not be lost after power-off.

When you start the system, the BIOS will perform a self-diagnostics test called Power On Self Test (POST) for all the attached devices, accessories, and the system. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

Note: Change the parameters when you fully understand their functions and subsequence.


AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.52
(C)2001 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Power Management Setup
PCI / Plug and Play Setup
Peripheral Setup
Hardware Monitor Setup
Auto-Detect Hard Disks
Change User Password
Change Supervisor Password
Auto Configuration with Optimal Settings
Auto Configuration with Fail Safe Settings
Save Settings and Exit
Exit Without Saving
Standard CMOS setup for changing time, date, hard disk type, etc.
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

BIOS Functions

On the menu, you can perform the following functions

1. Standard CMOS Setup
2. Advanced CMOS Setup
3. Advanced Chipset Setup
4. Power Management Setup
5. PCI/ Plug and Play Setup
6. Peripheral Setup
7. Hardware Monitor Setup
8. Auto-Detect Hard Disks
9. Change User Password
10. Change Supervisor Password
11. Auto Configuration with Optimal Settings: to auto configure the system according to optimal setting with pre-defined values. This is also the factory default setting of the system when you receive the board.
12. Auto Configuration with Fail Safe Settings: to configure the system in fail-safe mode with predefined values.
13. Save Settings and Exit: perform this function when you change the setting and exit the BIOS Setup program.
14. Exit without saving: perform this function when you want to exit the program and do not save the change.

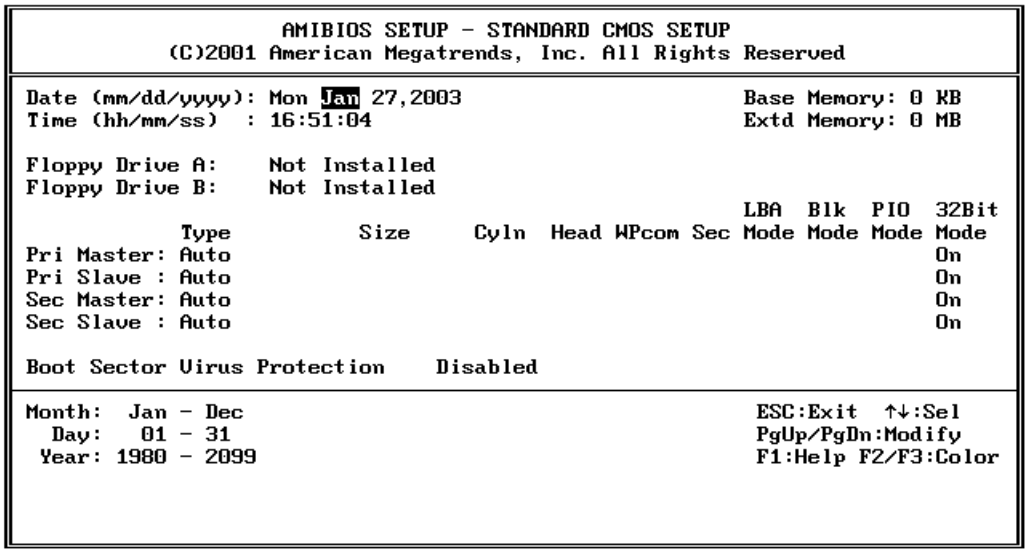
Keyboard Convention

On the BIOS, the following keys can be used to operate and manage the menu:

Item	Function
ESC	To exit the current menu or message
Page Up/Page Down	To select a parameter
F1	To display the help menu if you do not know the purpose or function of the item you are going to configure
F2/F3	To change the color of the menu display. F2 is to go forward and F3 is to go backward.
UP/Down Arrow Keys	To go upward or downward to the desired item

STANDARD CMOS SETUP

This section describes basic system hardware configuration, system clock setup and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.


AMIBIOS SETUP - STANDARD CMOS SETUP
(C)2001 American Megatrends, Inc. All Rights Reserved
Date (mm/dd/yyyy): Mon Jan 27,2003
Time (hh/mm/ss) : 16:51:04
Base Memory: 0 KB
Extd Memory: 0 MB
Floppy Drive A: Not Installed
Floppy Drive B: Not Installed
Type Size Cyln Head WPcom Sec LBA Mode Blk Mode PIO Mode 32Bit Mode
Pri Master: Auto On
Pri Slave : Auto On
Sec Master: Auto On
Sec Slave : Auto On
Boot Sector Virus Protection Disabled
Month: Jan - Dec
Day: 01 - 31
Year: 1980 - 2099
ESC:Exit ↑↓:Sel
PgUp/PgDn:Modify
F1:Help F2/F3:Color

- **Date & Time Setup**

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

- **Floppy Setup**

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

- **Hard Disk Setup**

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to four hard disks. For

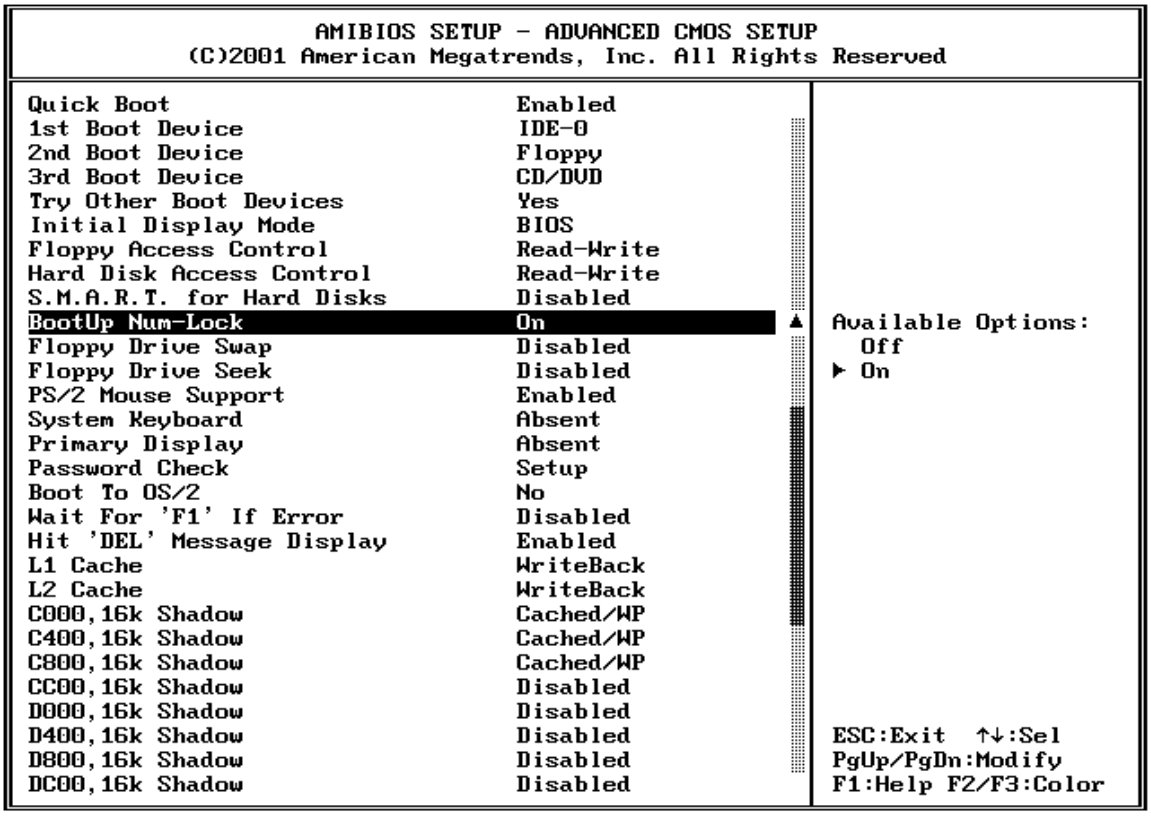
the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during boot up. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

- **Boot Sector Virus Protection**

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <***Disabled***>. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

ADVANCED CMOS SETUP



This section describes the configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

- **Quick Boot**

This field is used to activate the quick boot function of the system. When set to Enabled,

1. BIOS will not wait for up to 40 seconds if a Ready signal is not received from the IDE drive, and will not configure its drive.

2. BIOS will not wait for 0.5 seconds after sending a RESET signal to the IDE drive.

3. You cannot run BIOS Setup at system boot since there is no delay for the Hit, Del. To run Setup message.

Available Options: Disabled, Enabled

Default setting: Enabled

- **1st –3rd Boot Device**

These fields determine where the system attempts to look for the boot drive priority for an operating system. The default procedure is to check the hard disk, and then the floppy drive, and last the CDROM.

Available options: Disabled, IDE0-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CD/DVD, USB-FLOPPY, USB-CDROM, USB-HDD and SCSI, Network

Default setting: IDE-0 for 1st Boot device; Floppy for 2nd Boot Device; CDROM for 3rd Boot Device

- **Try Other Boot Device**

If all 3 1st –3rd boot devices specified by CMOS setup are not available to boot, BIOS will try to boot other available devices in following order if this question is set to "Enabled".

- **Initial Display Mode**

This field specifies can set Normal POST screen (BIOS) or Boot with logo, no POST messages (Client).

- **Floppy Access Control**

This field specifies the read/write access when booting from a floppy drive.

Available options: Normal, Read-only

Default setting: Normal

- **Hard Disk Access Control**

This field specifies the read/write access when booting from a HDD drive.

Available options: Normal, Read-only

Default setting: Normal

- **S.M.A.R.T for Hard Disk**

This field is used to activate the S.M.A.R.T (System Management and Reporting Technologies) function for S.M.A.R.T HDD drives. This function requires an application that can give S.M.A.R.T message.

Available options: Disabled, Enabled

Default: Disabled

- **Boot Up Num-lock**

This field is used to activate the Num Lock function upon system boot. If the setting is on, after a boot, the Num Lock light is lit, and user can use the number key.

Available options: On, Off

Default setting: On

- **Floppy Drive Swap**

The field reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the function's setting is <***Enabled***>, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Available options: Disabled, Enabled

Default setting: Disabled

- **Floppy Drive Seek**

This field is used to set if the BIOS will seek the floppy <A> drive upon boot.

Available Options: Disabled, Enabled

Default setting: Disabled

- **PS/2 Mouse Support**

The setting of ***Enabled*** allows the system to detect a PS/2 mouse on boot up. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. ***Disabled*** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

Available options: Disabled, Enabled

Default setting: Enable

- **System Keyboard**

This field specifies if an error message should be prompted when a keyboard is not attached.

Available options: Absent, Present

Default setting: Absent

- **Primary Display**

The field specifies the type of monitor installed in the system.

Available options: Absent, VGA/EGA, CGA40x25, CGA80x25, and Mono

Default setting: Absent

- **Password Check**

This field enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time and the BIOS Setup Program executes and the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Available options: Setup, Always

Default setting: Setup

- **Boot To OS2**

If OS2 operating system is used, and the system RAM is over 64MB, please select yes. Otherwise, select No.

Available options: Yes, No

Default setting: No

- **Wait for 'F1' If Error**

AMIBIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this field is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Available options: Disabled, Enabled

Default setting: Disabled

- **Hit 'DEL' Message Display**

Set this field to ***Disabled*** to prevent the message as follows:

```
Hit 'DEL' if you want to run setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Available options: Disabled, Enabled

Default setting: Enabled

- **C000, 32k Shadow - E800, 32k shadow**

These fields control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

1. **Disabled:** The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.

2. **Enabled:** The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.

3. **Cached/WP**: The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

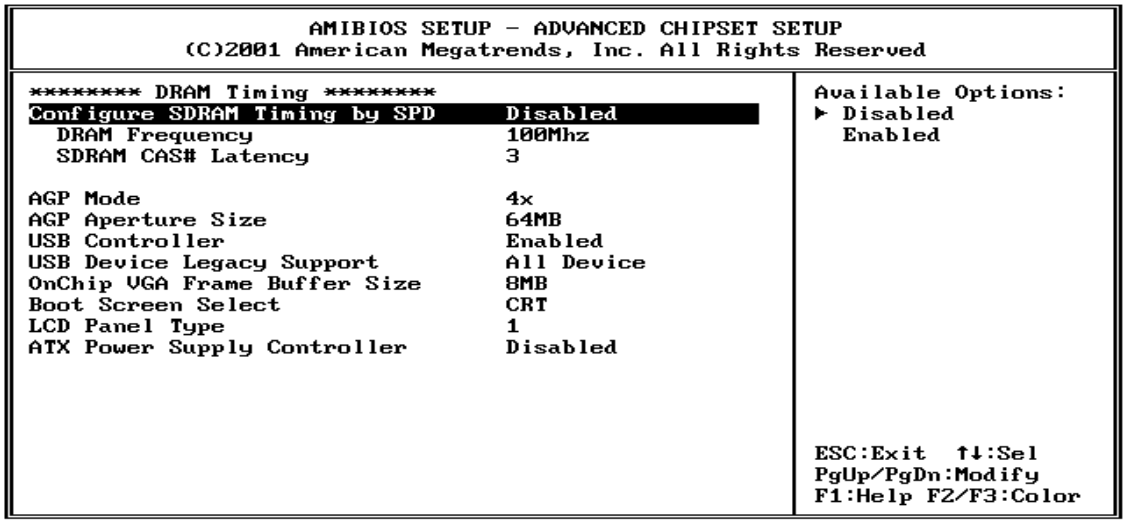
Available options: Disabled, Enabled, Cached

Default setting: Disabled

Default setting: Disable

ADVANCED CHIPSET SETUP

This section describes the configuration of the board's chipset features.



- **Configure SDRAM Timing by SPD**

SPD represents Serial Presence Detect. It is an 8-bit, 2048 bits EEPROM, built on the SDRAM for 100 MHz frequencies. If the installed SDRAM supports SPD function, select SPD. If not, you can select based on other access time of the SDRAM.

Available Options: Disabled, Enabled

Default setting: Disabled

- **DRAM Frequency**

This specifies the SDRAM memory clock frequency.

Available Options: 100MHz, 133MHz

Default setting: 100MHz

- **SDRAM CAS# Latency (SCLKs)**

This field specifies the latency for the Synchronous DRAM system memory signals.

Available Options: 3, 2

Default setting: 3

- **AGP Mode**

This field select AGP transfers video data.

Available Options: 1x, 2x and 4x

Default setting: 4x

- **AGP Aperture Size**

This field specifies the system memory size that can be used by the Accelerated Graphics Port (AGP).

Available Options: 4MB, 8MB, 16MB, 32MB, 64MB, 128MB and 256MB

Default setting: 64 MB

- **USB Control**

Select Enabled if a USB device is installed to the system. If Disabled are selected, the system will not be able to use a USB device.

Available Options: Disabled, Enabled

Default setting: Enabled

- **USB Device Legacy Support**

Select All Device if a USB device is installed to the system. If Disabled are selected, the system will not be able to use a USB device.

Available Options: Disabled, All Device

Default setting: All Device

- **OnChip VGA Frame Buffers Size**

This field is share memory architecture (SMA) for frame buffer memory. SMA allows system memory to be efficiently share by the host CPU and allocated depending on user preference, application requirements, and total size of system memory.

Available Options: None, 2MB, 4MB, 8MB, 16MB and 32MB

Default setting: 8 MB

Default setting: 8 MB

- **Boot Screen Select**

This field specifies which VGA display will be used when the system is boot. You can select either the LCD or the CRT booting on the VGA.

Available Options: Both, LCD, and CRT

Default setting: CRT

- **LCD Panel Type**

When use the LCD the field specifies which select display resolution for different TFT and STN LCD display type.

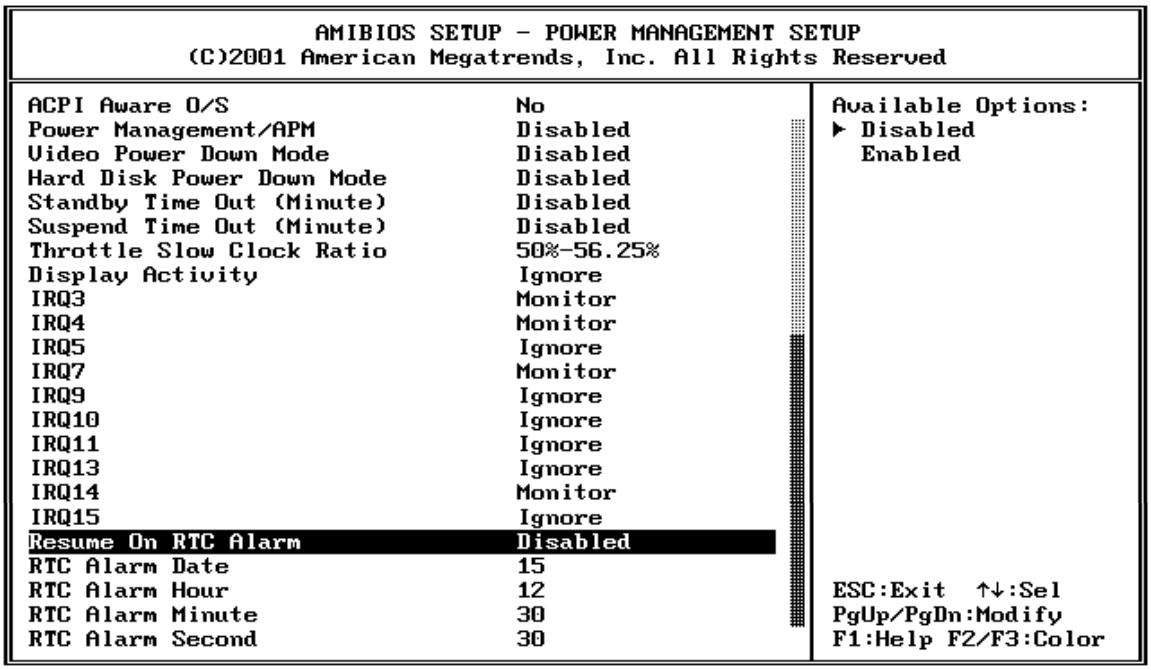
Available Options: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14 and 15

Default setting: 1

LCD Panel Type Table

Panel ID	Function	CN6	CN5
0	640x480	TFT	
1	800x600	TFT	LVDS
2	1024x768 2 Pixel/Clk at 32Mhz	TFT	
3	1280x1024	TFT	
4	640x480	DSTN	
5	800x600	DSTN	
6	1600x1200	TFT	LVDS
7	1024x768 1 Pixel/Clk at 65Mhz	TFT	
8	640x480	TFT	LVDS
9	800x600	TFT	
10	1024x768	TFT	
11	1280x1024	TFT	
12	1400x1050 2 Pixel/Clk at 54Mhz	TFT	
13	800x600	TFT	
14	1024x768	DSTN	
15	1280x1024	DSTN	

POWER MANAGEMENT



- **ACPI Aware O/S**

This filed specifies allow you enable Advanced Configuration and Power Management. When you use Windows/0S standby mode can set to enable.

Available Options: Disabled, Enabled

Default setting: Disable

- **Power Management /APM**

Select Enabled to activate the chipset Power Management and APM (Advanced Power Management) features.

Available Options: Disabled, Enabled

Default setting: Enabled

- **Video Power Down Mode**

This field specifies the power conserving state that video subsystem enters after the specified period of display inactivity has expired.

Available Options: Disabled, Standby, Suspend

Default setting: Disabled

- **Hard Disk Power Down Mode**

This field specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired.

Available Options: Disabled, Standby, Suspend

Default setting: Disabled

- **Standby Time Out (Minute)**

This field specifies the length of a period of system inactivity (like hard disk or video) while in full power on state. When this length of time expires, the system enters Standby power state.

Available Options: Disabled, 1 Minute, 2 Minute, 4 Minute, and 8 Minute, up to 60 Minute.

Default setting: Disabled

- **Suspend Time Out (Minute)**

This field specifies the length of a period of system inactivity (like hard disk or video) while in Standby state. When this length of time expires, the system enters Suspend power state.

Available Options: Disabled, 1 Minute, 2 Minute, 4 Minute, and 8 Minute, up to 60 Minute.

Default setting: Disabled

- **Throttle Slow Clock Ratio**

When the system enter Suspend or standby mode, the CPU clock runs only part of the time. You may select the percent of time that the clock runs.

Available Options: 0%-6.25, 25%37.5%, 75%87.5% and 93.75%-100%

Default setting: 50%-56.25%

- **IRQ3 ~IRQ15**

This field specifies the power down mode of the system based on the device. When the system does not receive signals from the device, it will enter the Power Down mode immediately. To enable the power saving mode, select Monitor. To disable it, select Ignore.

- **Resume On RTC Alarm**

This field specifies the RTC alarm to be turned off by extra software.

Available Options: Disabled, Enabled

Default setting: Disabled

- **RTC Alarm Date**

This field specifies the date of the RTC alarm.

Available Options: 1, 31

Default setting: 15

- **RTC Alarm Hour**

This field specifies the hour of the RTC alarm.

Available Options: 1-24

Default setting: 12

- **RTC Alarm Minute**

This field specifies the minute of the RTC alarm.

Available Options: 1-60

Default setting: 30

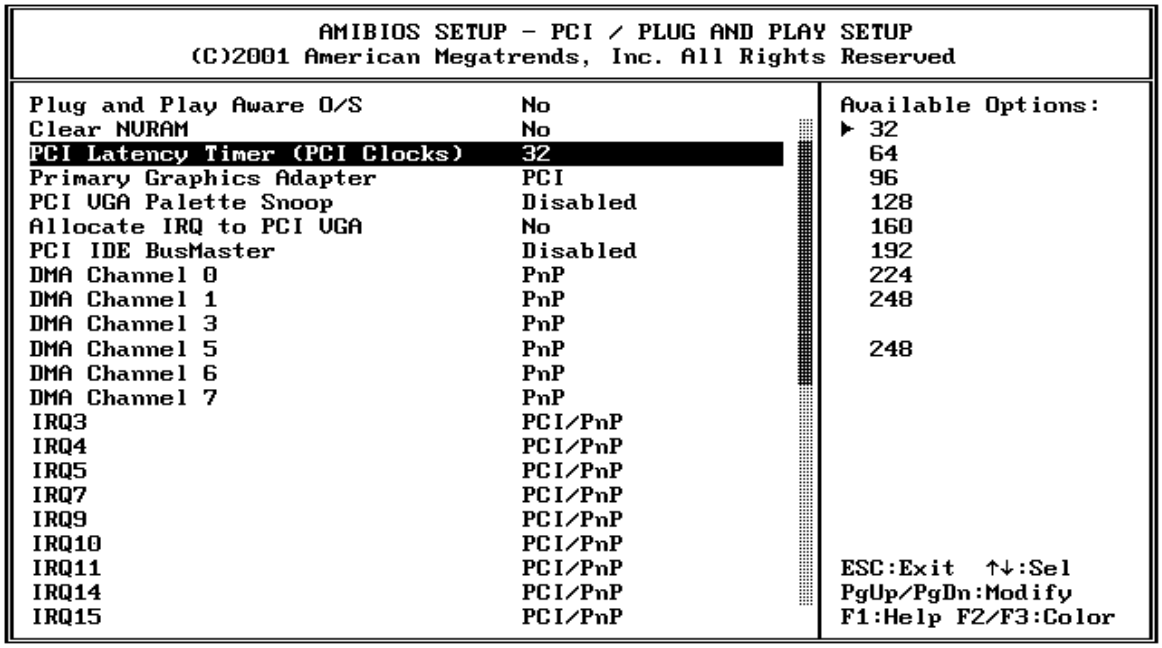
- **RTC Alarm Second**

This field specifies the second of the RTC alarm.

Available Options: 1-60

Default setting: 30

PCI/PLUG AND PLAY



- **Plug and Plug Aware O/S**

Set to Yes to inform BIOS that the operating system can handle Plug and Play (PnP) devices.

Available Options: Yes, No

Default setting: No

- **PCI Latency Timer**

This field specifies the latency timings (in PCI clock) PCI devices installed in the PCI expansion bus.

Available Options: 32, 64, 96, 128, 160,192, 224, and 248

Default setting: 64

- **Primary Graphics Adapter**

This field specifies which VGA display will be used when the system is boot. You can select either the onboard AGP or the VGA card installed on the PCI bus.

Available Options: AGP, PCI

Default setting: PCI

- **PCI VGA Palette Snoop**

When Enabled is selected, multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit. (0 is disabled).

Available Options:

Disabled: Data read and written by the CPU is only directed to the PCI VGA devices palette registers.

Enabled: Data read and written by the CPU is directed to both the PCI VGA devices palette registers.

Default setting: Disable

- **Allocate IRQ to PCI AGP**

When a PCI or AGP VGA device is installed, you can assign an IRQ to this device. Selecting Yes, BIOS will auto-assign IRQ to the device. Selecting No, no IRQ will be assigned to the VGA device.

Available Options: Yes, No

Default setting: No

- **PCI IDE BusMaster**

This option is to specify that the IDE controller on the PCI local bus have bus-mastering capability.

Available Options: Enable, Disable

Default setting: Disable

- **DMA Channel 0 – 7**

When I/O resources are controlled manually, you can assign each system DMA as one of the following types, based on the type of device using the interrupt:

ISA/EISA devices comply with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ5 for COM1).

PnP (PCI/ISA) devices: comply with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

Available Options: PnP, ISA/EISA

Default setting: PnP

- **IRQ 3 –15**

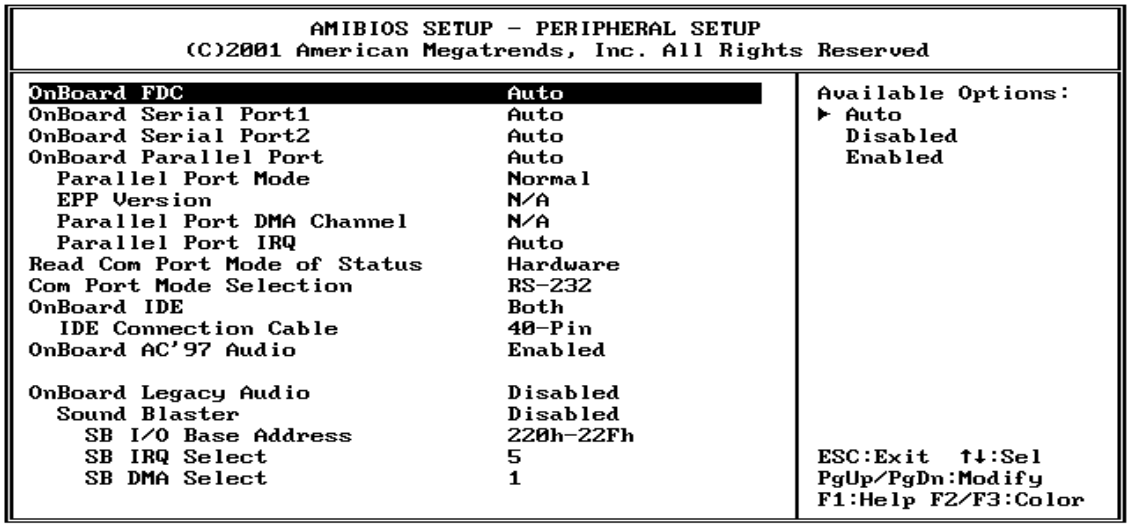
When I/O resources are controlled manually, you can assign each system interrupt as one of the following types, based on the type of device using the interrupt:

ISA/EISA devices comply with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ5 for COM1).

PnP (PCI/ISA) devices: comply with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

PERIPHERAL SETUP

This section describes the function of peripheral features.



- **OnBoard FDC**

This field enables the floppy drive controller on the FB2644.

Available Options: Disabled, Enabled and Auto

Default setting: Auto

- **OnBoard Serial Port 1**

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, and 3E8H/COM3, 2E8H/COM4.

Default setting: Auto

- **OnBoard Serial Port 2**

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, and 3E8H/COM3, 2E8H/COM4.

Default setting: Auto

- **OnBoard Parallel Port**

This field selects the I/O port address for parallel port.

Available Options: Auto, Disabled, 378, 278, and 3BCH

Default setting: Auto

- **EPP Version**

This field specifies the EPP version for the Parallel Port Mode specification used in the system and is not configurable. IF Normal or ECP is selected, this field displays N/A, meaning not available.

Available Options: N/A, 1.7, 1.9

Default setting: N/A

- **Parallel Port Mode**

This field specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications.

Available Options: N/A, Normal, Bi-Dir, EPP, and ECP

Default setting: Normal

- **Parallel Port IRQ**

This field specifies the IRQ for the parallel port.

Available Options: Auto, N/A, 5, 7

Default setting: Auto

- **Parallel Port DMA Channel**

This option is only available if the setting for the parallel Port Mode option is ECP.

Available Options: N/A, 0,1,3

Default setting: N/A

- **Read Com Port Mode of Status**

These fields are auto detected SW1-4 Setting, that can set use BIOS or adjust SW1.

Available Options: Software, Hardware

Default setting: Hardware

- **Com Port Mode Selection**

These fields item can select RS-232, RS-422, and RS-485 of Serial port 2.

Available Options: RS-232, RS-422 and RS-485

Default setting: RS-232

- **On-Chip IDE**

This field specifies the IDE channel that can be applied when using CN3 IDE hard disk connector.

Available Options: Disabled, Primary, and Secondary, Both

Default setting: Both

- **IDE Connection Cable**

This field specifies the select IDE use 40-pin or 40pin-80 conductor cable that can be applied when using UltraDMA/66/100 devices on CN3 IDE hard disk connector.

Available Options: 40-pin, 80-pin

Default setting: 40-pin

- **OnBoard AC'97 Audio**

This field specifies the internal Audio Control.

Available Options: Disable, Enable

Default setting: Enable

- **OnBoard AC'97 Modem**

This field specifies the internal Modem Control.

Available Options: Disable, Enable

Default setting: Enable

- **Sound Blaster**

This field if you want to use the SOUND Blaster emulation feature.

Available Options: Disable, Enable

Default setting: Disable

- **SB I/O Base Address**

These fields select the I/O port address for Audio.

Available Options: 220H~22FH, 240H~24FH, 260H~26FH and 280~28FH

Default setting: 220H~22FH

- **SB IRQ Select**

This field specifies the IRQ for the Audio.

Available Options: Disable, 5,7 and 10

Default setting: 5

- **SB DMA Select**

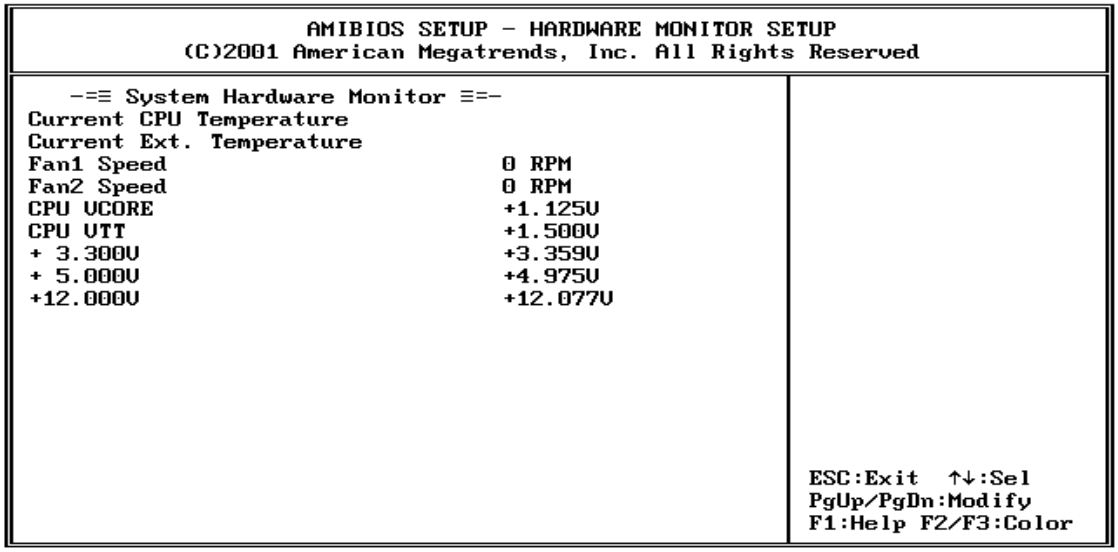
This field specifies the DMA for internal Audio Control.

Available Options: Disable, 0, 1,2 and 3

Default setting: 1

Hardware Monitor Setup

On the Hardware Monitor Setup screen, you can set up or monitor the system temperature, CPU voltage, and VIA C3 CPU Ration and CPU fan speed...



- **System Hardware Monitor**

  In this field, you can monitor or detect the followings items. These items are view-only and cannot be changed.
  - Current CPU Temperature
  - Current Ext. Temperature
  - Fan1 Speed
  - Fan2 Speed
  - CPU1 VCORE
  - CPU VTT
  - +3.300V
  - +5.000V
  - +12.00V

Password Setup

There are two security passwords: Supervisor and User. Supervisor is a privileged person that can change the User password from the BIOS.

According to the default setting, both access passwords are not set up and are only valid after you set the password from the BIOS.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password.**
2. Type the desired password (up to 8 character length) when you see the message, "Enter New Supervisor Password."
3. Then you can go on to set a user password (up to 8 character length) if required. Note that you cannot configure the User password until the Supervisor password is set up.
4. Enter Advanced CMOS Setup screen and point to the Password Checkup field.
5. Select Always or Setup.

✧ **Always:** a visitor who attempts to enter BIOS or operating system will be prompted for password.

✧ **Setup:** a visitor who attempts to the operating system will be prompted for user password. You can enter either User password or Supervisor password.

6. Point to **Save Settings and Exit** and press Enter.
7. Press Y when you see the message, "Save Current Settings and Exit (Y/N)?"

Note: it is suggested that you write down the password in a safe place to avoid that password may be forgotten or missing.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password**.
2. Press Enter instead of entering any character when you see the message, "Enter New Supervisor Password."
3. Thus you can disable the password.

Chapter 5 Driver and Utility

The enclosed diskette includes FB2644 VGA, Audio and LAN driver.

VGA/Audio Driver for WIN98/WIN95

Step 1: To install the VGA driver, insert the CD ROM into the CD ROM device, and enter DRIVER>VGA>Via8606>Win98_Me. If your system is not equipped with a CD ROM device, copy the VGA driver from the CD ROM to a 1.44" diskette.

Step 2: Open the Control Panel and double-click "SYSTEM" icon and then Click the "DEVICE Manager" Tab and double click "VGA Display".

Step 3: Click on DRIVE from the menu bar and new screen appears with the "Update Driver" button and then system will search VGA drive file starting form A: drive.

Step 4: As the installation is completed, the system will generate the message as follows.

Yes, I want to restart my computer now. Installation is done!

No, I will restart my computer later.

System must be restart then complete the installation.

Step 5: In the WINDOWS98/ME, you can find the <DISPLAYL> icon located in the {CONTROL PANEL} group.

Step 6: Adjust the <Refresh Rate>, <Font size> and <Resolution>.

Note: In the VGA/Audio/SysChip >Via8606>NT4.0, WINXP_2K directory, a Install.txt file is included to provide installation information

BIOS Flash Utility

In the <UTILITY> directory, there is the FLASH835.EXE file.

Step 1: Use the AMIFLASH.COM program to update the BIOS setting.

Step 2: And then refer to the chapter "BIOS Setup", as the steps to modify BIOS.

Step 3: Now the CPU board's BIOS loaded with is the newest program; user can use it to modify BIOS function in the future, when the BIOS add some functions.

LAN Utility

Step 1: To install the LAN utility OR driver, insert the CD ROM into the CD ROM device, and enter DRIVER>LAN>RTL8139C>DIAG. If your system is not equipped with a CD ROM device, copy the LAN VGA driver from the CD ROM to a 1.44" diskette.

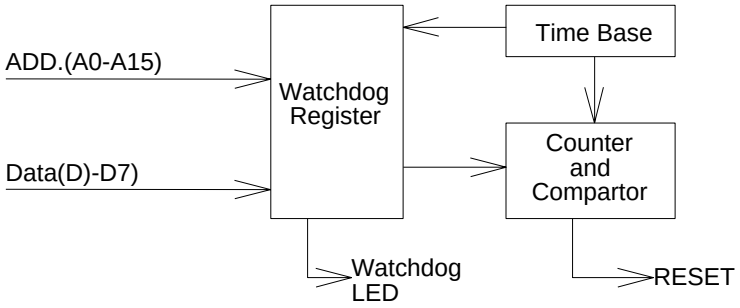
Step 2 Execute install.exe file.

Note: In the LAN directory, a HELPME.EXE file is included to provide installation information

Watchdog Timer

This section describes how to use the Watchdog Timer, including disabled, enabled, and trigger functions.

The FB2644 is equipped with a programmable time-out period watchdog timer. You can use your own program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger the I/O every time before the timer times out. If your program fails to trigger or disable this timer before it times out, e.g. because of a system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be set from 3 to 46 seconds.



Note: If you want to generate IRQ15 signal to warn your program when watchdog times out, the following table listed the relation of timer factors between time-out period. And if you use the IRQ15 signal to warn your program when watchdog timer out, please enter the BIOS Setup the <Peripheral Setup> menu, the <OnBoard PCI IDE> and <IDE Prefetch> these two items must set to *Primary*.

Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect system crashes or hang-ups. LED1 on this CPU board is the watchdog timer indicator, which is located at the upper-left corner above the USB connector. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times out. After you trigger the watchdog timer, it will be set to non-zero value to watchdog counter and start to count down again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system.

The factor of the watchdog timer time-out constant is approximately 6 seconds. The period for the watchdog timer time-out period is between 1 to 8 timer factors.
If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out periods.

Reset Time Factor	IRQ 11 Time Factor	IRQ 15 Time Factor	Time-Out Period (Sec)
20h	38h	30h	3
21h	39h	31h	9
22h	3Ah	32h	15
23h	3Bh	33h	22
24h	3Ch	34h	28
25h	3Dh	35h	34
26h	3Eh	36h	40
27h	3Fh	37h	46

Note:

1. If you program the watchdog to generate IRQ15 signal when it times out, you should initial IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too.
2. Before you initial the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer previously; otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog register whose address is 76H. The following is a BASICA program, which demonstrates how to enable the watchdog timer and set the time-out period at 28 seconds.

```
1000        REM Points to command register
1010        WD_REG% = 76hH
1020        REM Timer factor = 24H (or 34H)
1030        TIMER_FACTOR% = %H24
1040        REM Output factor to watchdog register
1050        OUT WD_REG%, TIMER_FACTOR%
```

Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in next trigger. Below is a BASICA program, which demonstrates how to trigger the watchdog timer:

```
2000        REM Points to command register
2010        WD_REG% = 76H
2020        REM Timer factor = 76H (or 34H)
2030        TIMER_FACTOR% = &H76
2040        REM Output factor to watchdog register
2050        OUT WD_REG%, TIMER_FACTOR%
        . Etc.
```

Watchdog Timer Disabled

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
3000        REM Points to command register
3010        WD_REG% = BASE_PORT%
3020        REM Timer factor = 0
3030        TIMER_FACTOR% = 0
3040        REM Output factor to watchdog register
3050        OUT WD_REG%, TIMER_FACTOR%
        . Etc.
```

Programming RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 precedes the transmission, which needs control the TXC signal, and the installing, steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

Note: Please refer to the section of the "Serial Ports" in the Chapter "System Controllers" for the detail description of the COM port's register.

❑ **Initialize COM port**

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

NOTE: Control the FB2644 CPU card's DTR signal to the RS-485's TXC communication.

❑ **Send out one character (Transmit)**

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

❑ **Send out one block data (Transmit – the data more than two characters)**

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

- **Receive data**

The RS-485's operation of receiving data is in the same of the RS-232's.

- **Basic Language Example**

a. Initial 86C450 UART

```
10      OPEN "COM1:9600,m,8,1"AS #1 LEN=1
20      REM Reset DTR
30      OUT &H3FC, (INP(%H3FC) AND &HFA)
40      RETURN
```

b. Send out one character to COM1

```
10      REM Enable transmitter by setting DTR ON
20      OUT &H3FC, (INP(&H3FC) OR &H01)
30      REM Send out one character
40      PRINT #1, OUTCHR$
50      REM Check transmitter holding register and shift register
60      IF ((INP(&H3FD) AND &H60) >0) THEN 60
70      REM Disable transmitter by resetting DTR
80      OUT &H3FC, (INP(&H3FC) AND &HEF)
90      RETURN
```

- **c. Receive one character from COM1**

```
10      REM Check COM1: receiver buffer
20      IF LOF(1)<256 THEN 70
30      REM Receiver buffer is empty
40      INPSTR$"
```

```
50      RETURN

60      REM Read one character from COM1: buffer

70      INPSTR$=INPUT$(1,#1)

80      RETURN
```

NOTE: The example of the above program is based on COM1 (I/O Address 3F8h). The RS-485 of the FB2644 uses COM2. If you want to program it, please refer to the BIOS Setup for COM2 address setup.

Chapter 6 Technical Reference

This section outlines the errors that may occur when you operate the system, and also gives you the suggestions on solving the problems.

Topic include:

- Trouble Shooting for Error Messages
- Technical Reference

Trouble Shooting for Error Messages

The following information informs the error messages and troubleshooting. Please adjust your systems according to the messages below. Make sure all the components and connectors are in proper position and firmly attached. If the errors still exist, please contact with your distributor for maintenance.

❑ **POST BEEP**

Currently there are two kinds of beep codes in BIOS setup.

- One indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by three short beeps.
- The other indicates that an error has occurred in your DRAM. This beep code consists of a constant single long beep.

❑ **CMOS BATTERY FAILURE**

When the CMOS battery is out of work or has run out, the user has to replace it with a new battery.

- **CMOS CHECKSUM ERROR**

This error informs that the CMOS has corrupted. When the battery runs weak, this situation might happen. Please check the battery and change a new one when necessary.

- **DISPLAY SWITCH IS SET INCORRECTLY**

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in BIOS Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter BIOS Setup and change the video selection.

- **DISK BOOT FAILURE**

When you can't find the boot device, insert a system disk into Drive A and press < Enter >. Make sure both the controller and cables are all in proper positions, and also make sure the disk is formatted. Then reboot the system.

- **DISKETTE DRIVES OR TYPES MISMATCH ERROR**

When the diskette drive type is different from CMOS, please run setup or configure the drive again.

- **ERROR ENCOUNTERED INITIALIZING HARD DRIVE**

When you can't initialize the hard drive, ensure the following things:

1. The adapter is installed correctly
2. All cables are correctly and firmly attached
3. The correct hard drive type is selected in BIOS Setup

- **ERROR INITIALIZING HARD DISK CONTROLLER**

When this error occurs, ensure the following things:

1. The cord is exactly installed in the bus.
2. The correct hard drive type is selected in BIOS Setup
3. Whether all of the jumpers are set correctly in the hard drive

- **FLOPPY DISK CONTROLLER ERROR OR NO CONTROLLER PRESENT**

When you cannot find or initialize the floppy drive controller, please ensure the controller is in proper BIOS Setup. If there is no floppy drive installed, ensure the Diskette Drive selection in Setup is set to NONE.

- **KEYBOARD ERROR OR NO KEYBOARD PRESENT**

When this situation happens, please check keyboard attachment and no keys being pressed during the boot. If you are purposely configuring the system without a keyboard, set the error halt condition in BIOS Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot procedure.

- **MEMORY ADDRESS ERROR**

When the memory address indicates error. You can use this location along with the memory map for your system to find and replace the bad memory chips.

- **MEMORY SIZE HAS CHANGED**

Memory has been added or removed since last boot. In EISA mode, use Configuration Utility to re-configure the memory configuration. In ISA mode enter BIOS Setup and enter the new memory size in the memory fields.

- **MEMORY VERIFYING ERROR**

It indicates an error verifying a value is already written to memory. Use the location along with your system's memory map to locate the bad chip.

- **OFFENDING ADDRESS MISSING**

This message is used in connection with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

- **REBOOT ERROR**

When this error occurs that requires you to reboot. Press any key and the system will reboot.

- **SYSTEM HALTED**

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

Technical Reference

Real-Time Clock and Non-Volatile RAM

The FB2644 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed below:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte

Address	Description
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

CMOS RAM Map

Register	Description
00h -10h	Standard AT-compatible RTC and Status and Status Register data definitions
11h – 13h	Varies
14h	Equipment Bits 7-6 Number of Floppy Drives 00 1 Drive 01 2 Drives Bits 5-4 Monitor Type 00 Not CGA or MDA 01 40x25 CGA 01 2 Drives 80x25 CGA Bits 3 Display Enabled 0 Disabled 1 Enabled Bit 2 Keyboard Enabled 00 Not CGA or MDA 01 40x25 CGA 01 2 Drives 80x25 CGA Bit 1 Math Coprocessor Installed 0 Absent 1 Present Bit 0 Floppy Drive Installed 0 Disabled 1 Enabled
15h	Base Memory (in 1KB increments), Low Byte
16h	Base Memory (in 1KB increments), High Byte
17h	IBM-compatible memory (in 1KB increments), Low Byte
18h	IBM-compatible memory (in 1KB increments), High Byte (max 15 MB)
19h-2Dh	Varies
2Eh	Standard CMOS RAM checksum, high byte
2Fh	Standard CMOS RAM checksum, low byte
30h	IBM-compatible Extended Memory, Low Byte (POST) in KB
31h	IBM-compatible Extended Memory, High Byte (POST) in KB
32h	Century Byte
33h	Reserved. Do not use
34h	Reserved. Do not use
35h	Low byte of extended memory (POST) in 64 KB
36h	High byte of extended memory (POST) in 64 KB
37h-3Dh	Varies
3Eh	Extended CMOS Checksum, Low Byte (including 34h-3Dh)
3Fh	Extended CMOS Checksum, High Byte (including 34h-3Dh)

I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses, which also becomes the identity of the device. There is a total of 1K-port address space available. The following table lists the I/O port addresses used on the Industrial CPU Card.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h - 0FFh	Math Coprocessor
1F0h - 1F7h	IDE Interface
278h - 27Fh	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
378h - 3FFh	Parallel Port #1(LPT1)
3B0h - 3BFh	Monochrome & Printer adapter
3C0h - 3CFh	EGA adapter
3D0h - 3DFh	CGA adapter
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)
400h - 40Fh	Plug & Play PCI Bus
4D5h - 4D1h	Plug & Play PCI Bus
800h - 87Fh	Plug & Play PCI Bus
880h - 88Fh	Plug & Play PCI Bus
C00h - CFFh	Plug & Play PCI Bus
CF8h - CFFh	Plug & Play PCI Bus
E800h - E8FEh	Ethernet Controller
EC00h - EC1Eh	USB Controller
FC00h – FC0Eh	IDE Controller

Interrupt Request Lines (IRQ)

There are a total of 15 IRQ lines available on the Industrial CPU Card. Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on the Industrial CPU Card.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	USB
IRQ11	Ethernet
IRQ12	PS2 Mouse
IRQ13	Math coprocessor
IRQ14	Primary IDE
IRQ15	Secondary IDE

DMA Channel Map

The equivalent of two 8237A DMA controllers are implemented in the FB2644 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speeding information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: Reserved for IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Serial Ports

The ACEs (Asynchronous Communication Elements ACE1 to ACE2) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

DLAB	Port Address	Register
0	Base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	Base + 1	Interrupt enable
X	Base + 2	Interrupt identification (read only)
X	Base + 3	Line control
X	Base + 4	MODEM control
X	Base + 5	Line status
X	Base + 6	MODEM status
X	Base + 7	Scratched register
1	Base + 0	Divisor latch (least significant byte)
1	Base + 1	Divisor latch (most significant byte)

- **Receiver Buffer Register (RBR)**

Bit 0-7: Received data byte (Read Only)

- **Transmitter Holding Register (THR)**

Bit 0-7: Transmitter holding data byte (Write Only)

- **Interrupt Enable Register (IER)**

Bit 0: Enable Received Data Available Interrupt (ERBFI)

Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)

Bit 2: Enable Receiver Line Status Interrupt (ELSI)

Bit 3: Enable MODEM Status Interrupt (EDSSI)

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

- **Interrupt Identification Register (IIR)**

Bit 0: "0" if Interrupt Pending

Bit 1: Interrupt ID Bit 0

Bit 2: Interrupt ID Bit 1

Bit 3: Must be 0

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

- **Line Control Register (LCR)**

Bit 0: Word Length Select Bit 0 (WLS0)

Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)

Bit 3: Parity Enable (PEN)

Bit 4: Even Parity Select (EPS)

Bit 5: Stick Parity

Bit 6: Set Break

Bit 7: Divisor Latch Access Bit (DLAB)

- **MODEM Control Register (MCR)**

Bit 0: Data Terminal Ready (DTR)

Bit 1: Request to Send (RTS)

Bit 2: Out 1 (OUT 1)

Bit 3: Out 2 (OUT 2)

Bit 4: Loop

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

- **Line Status Register (LSR)**

Bit 0: Data Ready (DR)

Bit 1: Overrun Error (OR)

Bit 2: Parity Error (PE)

Bit 3: Framing Error (FE)

Bit 4: Break Interrupt (BI)

Bit 5: Transmitter Holding Register Empty (THRE)

Bit 6: Transmitter Shift Register Empty (TSRE)

Bit 7: Must be 0

- **MODEM Status Register (MSR)**

Bit 0: Delta Clear to Send (DCTS)

Bit 1: Delta Data Set Ready (DDSR)

Bit 2: Training Edge Ring Indicator (TERI)

Bit 3: Delta Receive Line Signal Detect (DSLSD)

Bit 4: Clear to Send (CTS)

Bit 5: Data Set Ready (DSR)

Bit 6: Ring Indicator (RI)

Bit 7: Received Line Signal Detect (RSLD)

- **Divisor Latch (LS, MS)**

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Parallel Ports

- **Register Address**

Port Address	Read/Write	Register
Base + 0	Write	Output data
Base + 0	Read	Input data
Base + 1	Read	Printer status buffer
Base + 2	Write	Printer control latch

- **Printer Interface Logic**

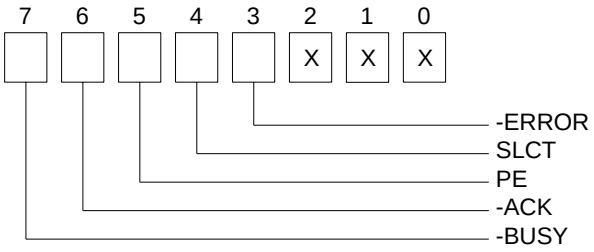
The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

- **Data Swapper**

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address

- **Printer Status Buffer**

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described below:



NOTE: X represents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

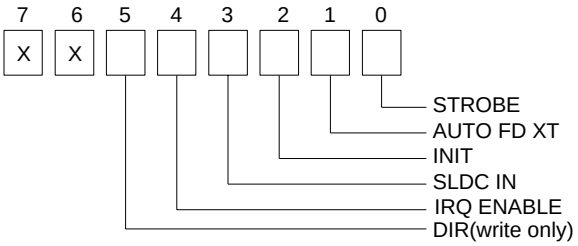
Bit 5: A 1 means the printer has detected the end of the paper.

Bit 4: A 1 means the printer is selected.

Bit 3: A 0 means the printer has encountered an error condition.

- **Printer Control Latch & Printer Control Swapper**

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:



NOTE: X represents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write-only.

Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A 1 in this bit position selects the printer.

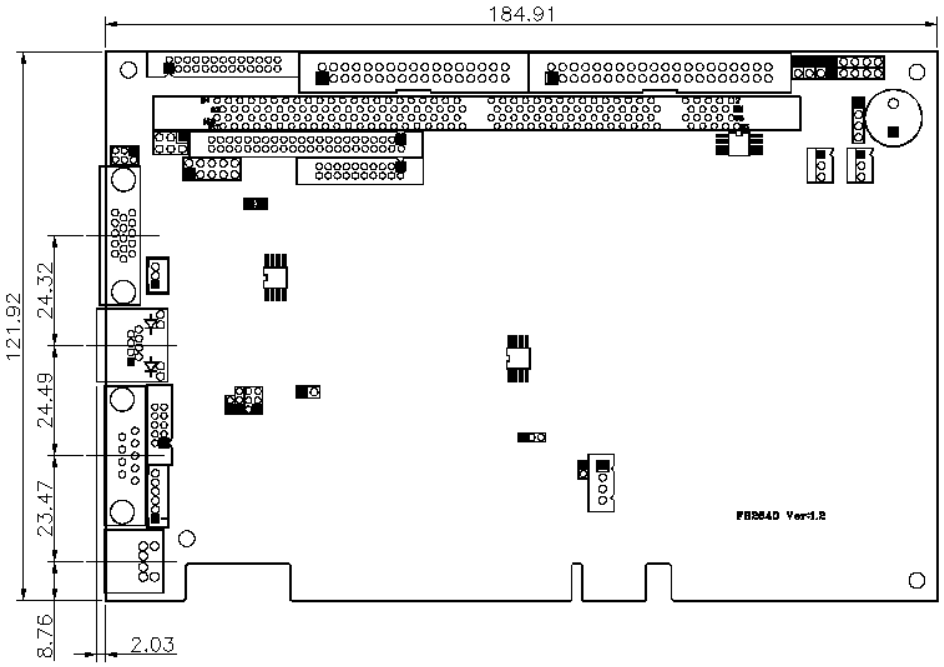
Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

Appendix

Dimension

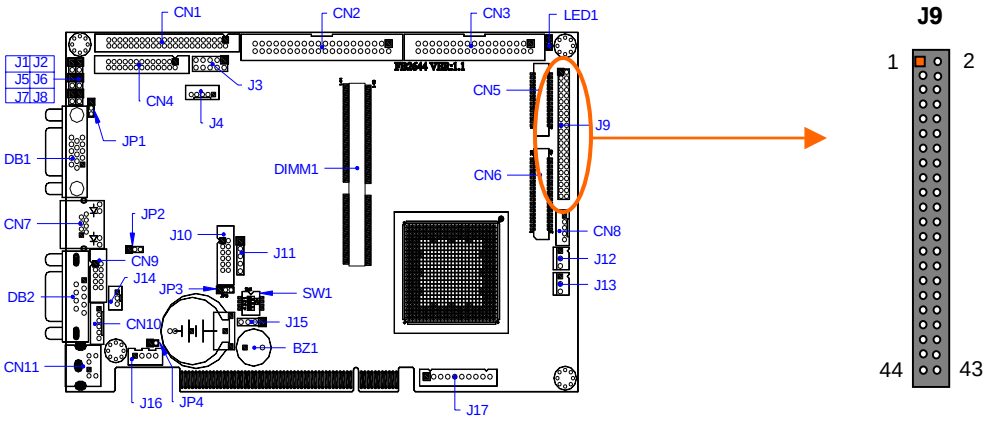


Unit: mm

Special Features

□ J9: Feature Connector (J9: 44-pin 2.0mm IDC)

J9 is a feature connector and which supports signals for Video In/Out solutions. All of these functions consist in FB4644 adapter board (optional). The following table lists the pin definitions of J9 connector:



J9	Description	J9	Description
1	+5V	2	+5V
3	ZVHS	4	ZWS
5	ZVCLK	6	Ground
7	ZVD0	8	ZVD1
9	ZVD2	10	ZVD3
11	ZVD4	12	ZVD5
13	ZVD6	14	ZVD7
15	ZVD8	16	ZVD9
17	ZVD10	18	ZVD11
19	ZVD12	20	ZVD13
21	ZVD14	22	ZVD15
23	SPDAT	24	SPCLK
25	Ground	26	TVD0/FP28
27	TVD1/FP29	28	TVD2/FP33
29	TVD3/FP30	30	TVD4/FP25
31	TVD5/FP26	32	TVD6/FP24
33	TVD7/FP27	34	TVD8
35	TVD9	36	TVD10
37	TVD11	38	TVBLK#
39	TVHS/FP34	40	TWS/FP31
41	GOP0	42	TVCLK/FP32
43	Ground	44	TVCLKR/FP35

Note *1:These signals also are used to corporate with CN6 for connecting 36-bit TTL LCD panels.